VadaTech UTC001 / UTC002

Hardware Reference Manual

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Revision History

Doc Rev	Description of Change	Revision Date
1.0.0	Document Created (for UTC001)	03/09/2009
2.0.0	UTC002 description added.	07/12/2010
2.1.0	Updated front panel diagrams/descriptions. Added currently available fabric board daughter card descriptions.	03/26/2013

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Tables

1 Overview

The UTC001 and UTC002 are feature-rich MicroTCA Carrier Hub (MCH) modules based on the MicroTCA (µTCA) specification. They provide complete µTCA Carrier Management Controller (MCMC) as well as an optional Shelf Manager functionality. They come with a 1GbE (L2 Managed) switch fabric option with an optional SAS/SATA Expander plus one additional optional fabric for PCIe (Gen2 x4), SRIO (x4), 10GbE (L2 Managed), or Cross Bar Switch (CBS). PCIe clock generation with or without Spread Spectrum Clocking is optionally available. The UTC001 also provides optional Telco clock distribution and synchronization with Stratum 3 holdover via Telecom, GPS synchronized clocking, or clock routing only options. The UTC001 and UTC002 are very similar products at their core but they differ in terms of their front panel I/O capabilities and in the Ethernet connectivity between the 1GbE and 10GbE switches. These differences will be explained further in subsequent sections.

As a hot-swappable field replaceable unit (FRU), the UTC001/UTC002 follows a stringent carrier grade feature set to provide Reliability, Availably, Serviceability and Maintainability (RASM). The UTC001/UTC002 supports a redundant configuration with two UTC001's or two UTC002's in the same chassis with automatic failover. When two UTC001/UTC002's are used in a chassis, advanced high-speed fabric combinations are supported such as PCIe + 10GbE.

The software is IPMI 2.0 Compliant and can also be ordered as a protocol analyzer to aid in system integration/debugging (ordering option 'A' determines the software load for MCMC only, MCMC and Shelf Manager, or Protocol Analyzer).

1.1 About This Manual

The UTC001/UTC002 reference manual provides functional, architectural, and mechanical descriptions of the UTC001 and UTC002 modules. This manual is intended for anyone who designs OEM products which have requirements for an MCH to provide chassis/shelf management, switch fabrics, and/or Telco clocking.

The UTC001/UTC002 design is highly modular and includes various mount options and daughter cards. These options are exposed as ordering options in the UTC001/UTC002 Datasheets. These ordering options are mentioned in the remainder of this manual such as 'E = 3' to explain how the ordering options affect the hardware functionality. Please refer to the last page of the UTC001/UTC002 Datasheets for a list of these options. They generally take the form of 'UTC001/2-ABC-DEF-GHJ'. The letters are replaced by numbers selected from the lists of available options. Please keep your model number handy when reviewing

the remainder of this document so that you can keep your module's particular configuration in mind.

1.1.1 Feedback

VadaTech welcomes feedback about how we can make our manuals and technical documentation more useful to our customers. Please feel free to send comments and suggestions to support@vadatech.com.

1.1.2 Document References

- VadaTech UTC001 and UTC002 Datasheets
- VadaTech MicroTCA MCH Getting Started Guide (& related software documents)
- VadaTech Gigabit Ethernet Managed Switch Setup Guide
- VadaTech Gigabit Ethernet Switch Web Interface Reference Manual
- VadaTech 10GbE Switch User Guide
- VadaTech 10GbE Switch CLI Reference Manual
- VadaTech 10GbE Switch Diagnostics/Low-Level Commands Manual
- PICMG uTCA Specification
- PICMG AMC Specifications
- PICMG ATCA Specification
- IPMI Specification

1.2 Acronyms Used in this Document

Acronym	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
FRU	Field Replaceable Unit
GbE	Gigabit Ethernet
GPS	Global Positioning System
I-PASS	Infiniband (connector)
IPMI	Intelligent Platform Management Interface
L2	Layer 2 (i.e. Link Layer)
L3	Layer 3 (i.e. IP Layer)
MCH	MicroTCA Carrier Hub
MCMC	MicroTCA Carrier Management Controller
PCIe	Peripheral Component Interconnect Express
SAS	Serial Attached SCSI

SATA	Serial AT Attachment
SMA	SubMiniature Version A (connector)
SRIO	Serial Rapid I/O
TCXO	Temperature Compensated Crystal Oscillator
*u*TCA	MicroTCA
VCTCXO	Voltage Controlled Temperature Compensated Crystal Oscillator
XAUI	10 Gigabit Attachment Unit Interface

Table 1: Acronyms

2 UTC001 Mechanical Description

The UTC001 is a µTCA Carrier Hub (full-height) measuring 180.6 mm by 73.5 mm. The UTC001 module is made up of several boards; the UTC001 base board, the VT002 IPMI Controller board, and an optional high-speed fabric board which is one of DA111 (PCIe Gen2), DA112 (10GbE), DA113 (SRIO Gen1), DA115 (PCIe Gen2 w/ switch partitioning), or DA132 (CBS). The following figures show the component side layouts of these boards:

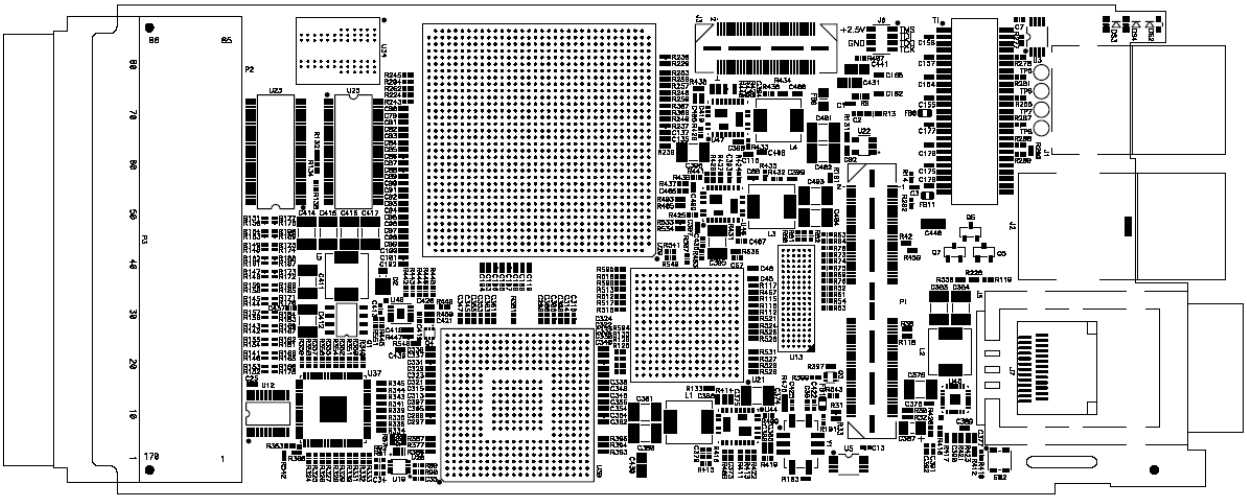

Figure 1: UTC001 (Base board) component side layout

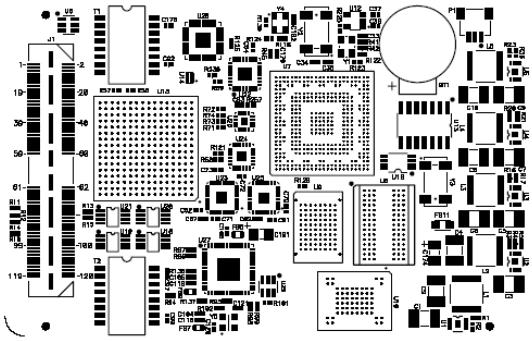

Figure 2: VT002 (IPMI Controller) component side layout

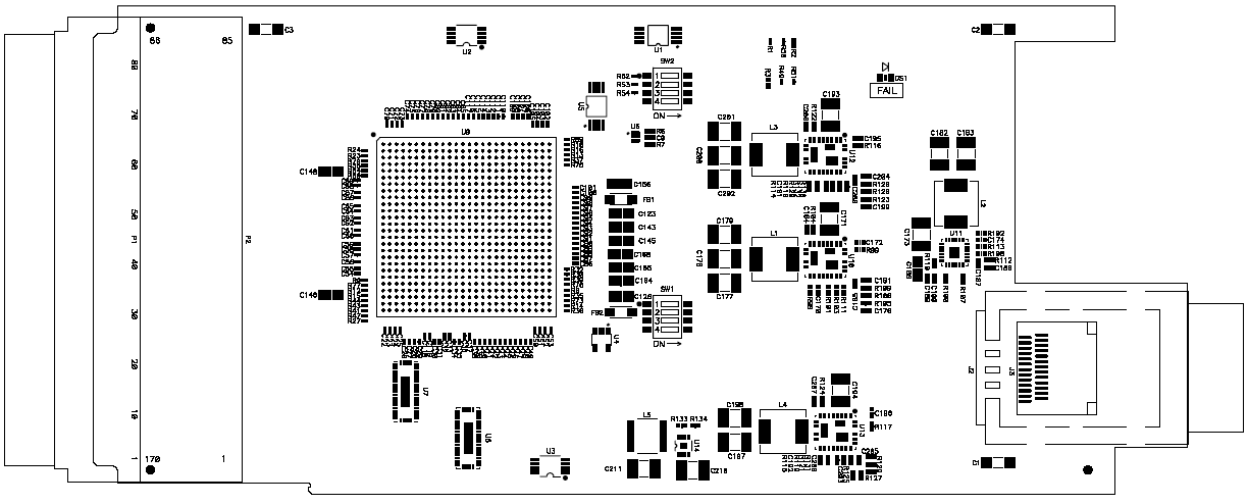

Figure 3: DA111 (PCIe Fabric) component side layout

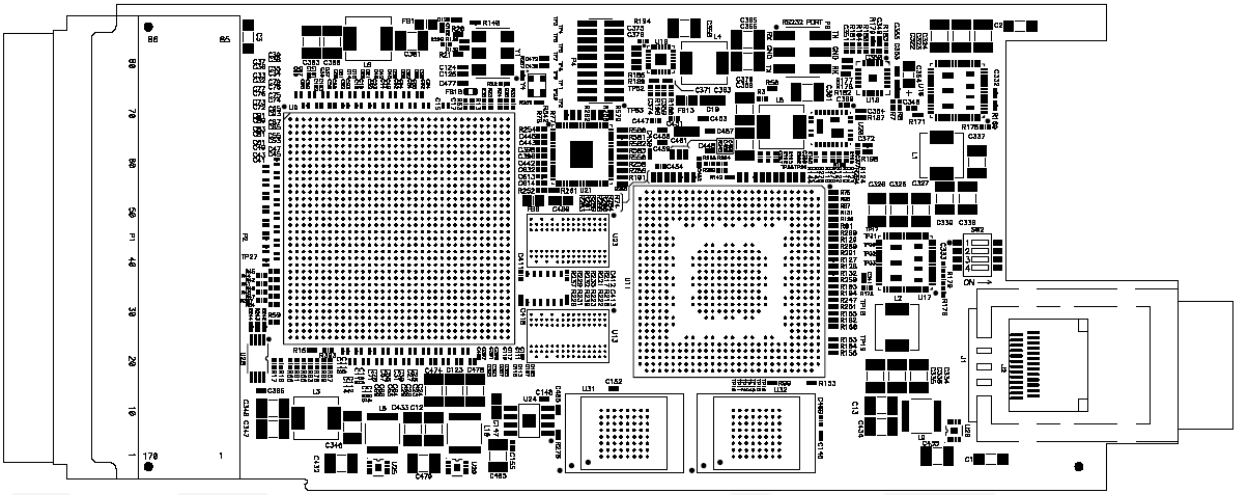

Figure 4: DA112 (10GbE Fabric) component side layout

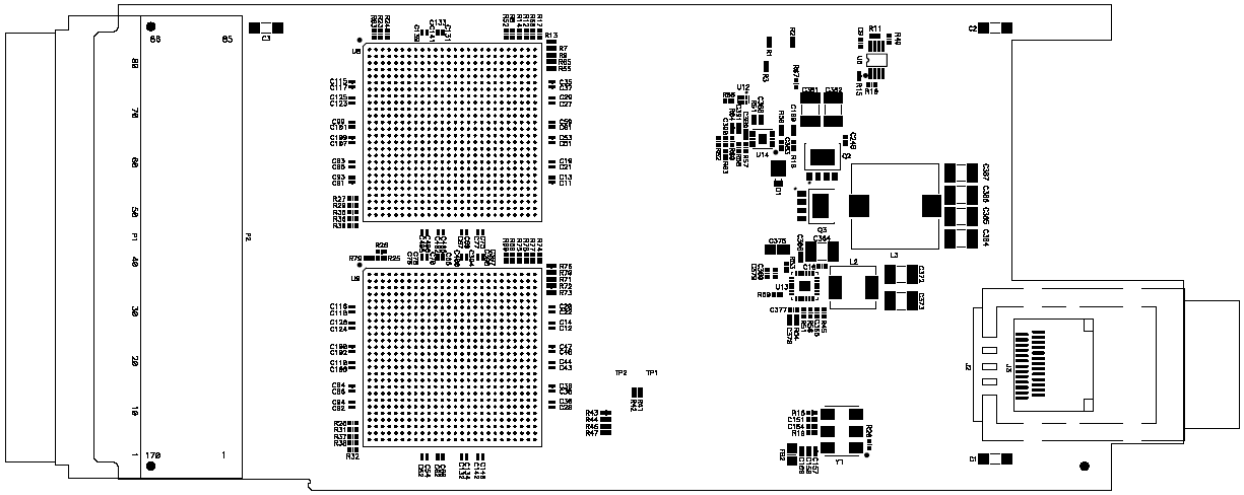

Figure 5: DA113 (SRIO Fabric) component side layout

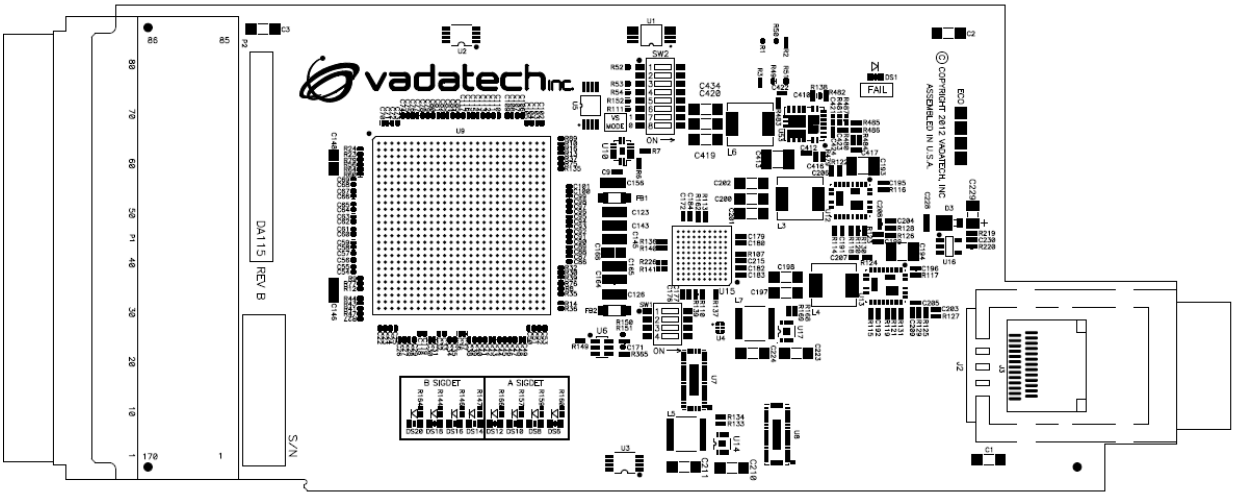

Figure 6: DA115 (PCIe Fabric w/ Switch Partitioning) component side layout

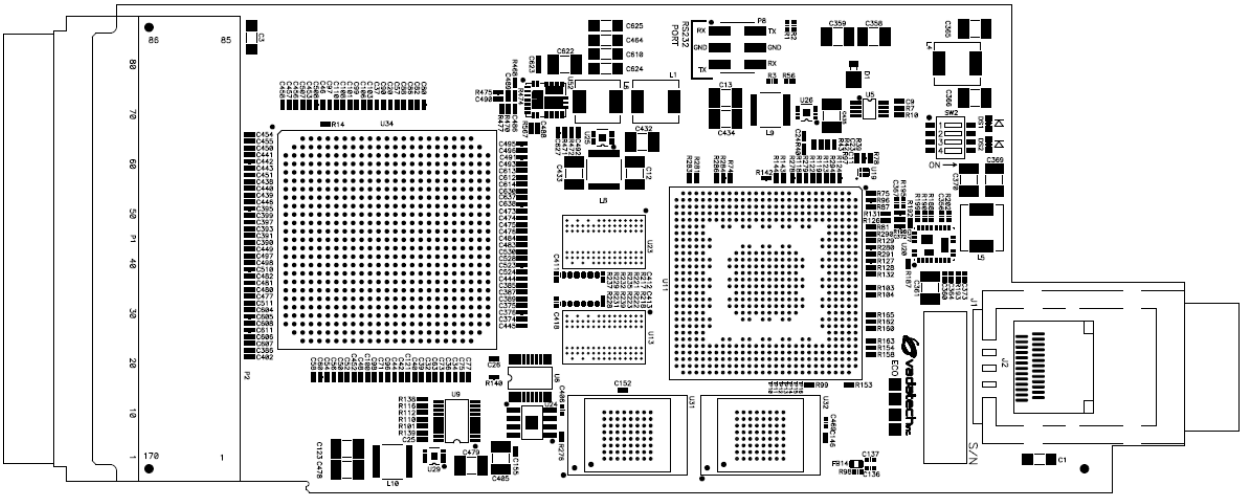

Figure 7: DA132 (CBS) component side layout

3 UTC002 Mechanical Description

The UTC002 is a µTCA Carrier Hub (full-height) measuring 180.6 mm by 73.5 mm. The UTC002 module is made up of several boards; the UTC002 base board, the VT002 IPMI Controller board, and an optional high-speed fabric board such as DA116 (10GbE), DA117 (PCIe Gen2), DA118 (SRIO Gen1), DA133 (SRIO Gen2), DA134 (CBS), or DA002 (Clock I/O only). The following figures show the component side layouts of these boards:

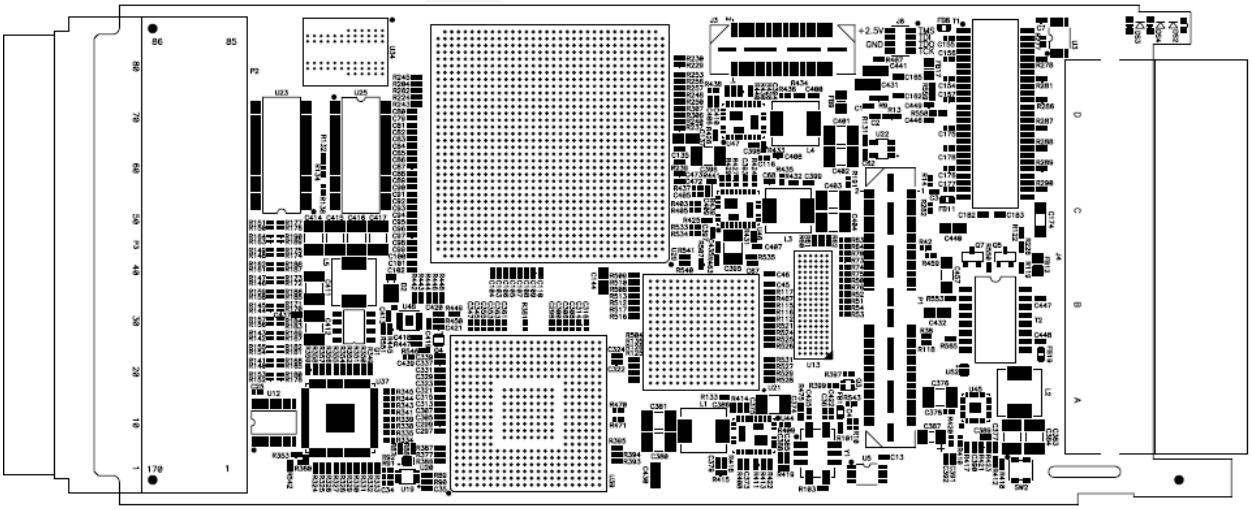

Figure 8: UTC002 (Base board) component side layout

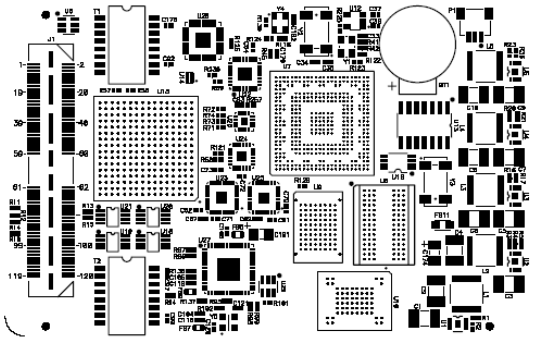

Figure 9: VT002 (IPMI Controller) component side layout

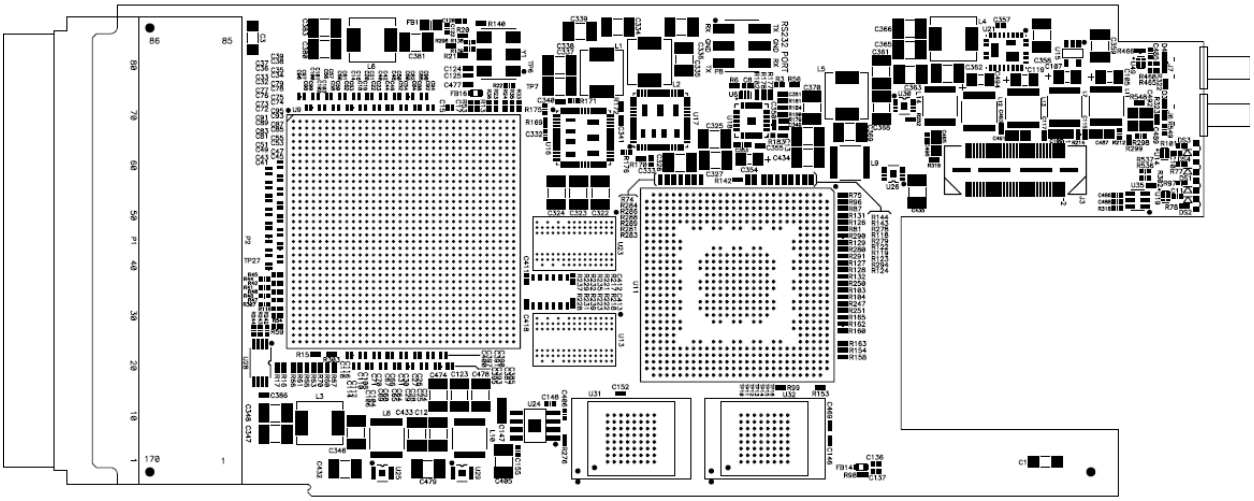

Figure 10: DA116 (10GbE Fabric) component side layout

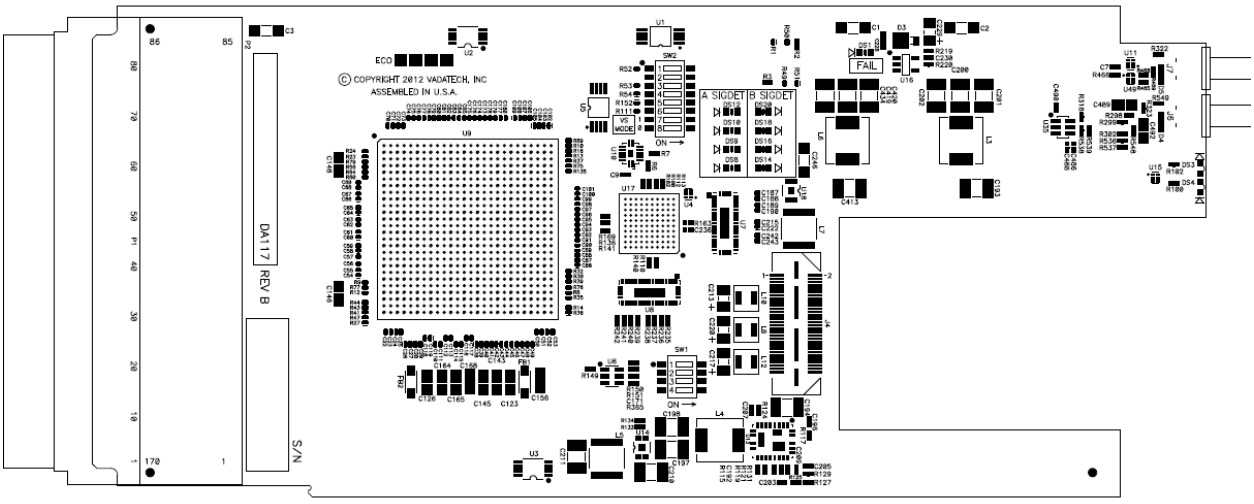

Figure 11: DA117 (PCIe Fabric) component side layout

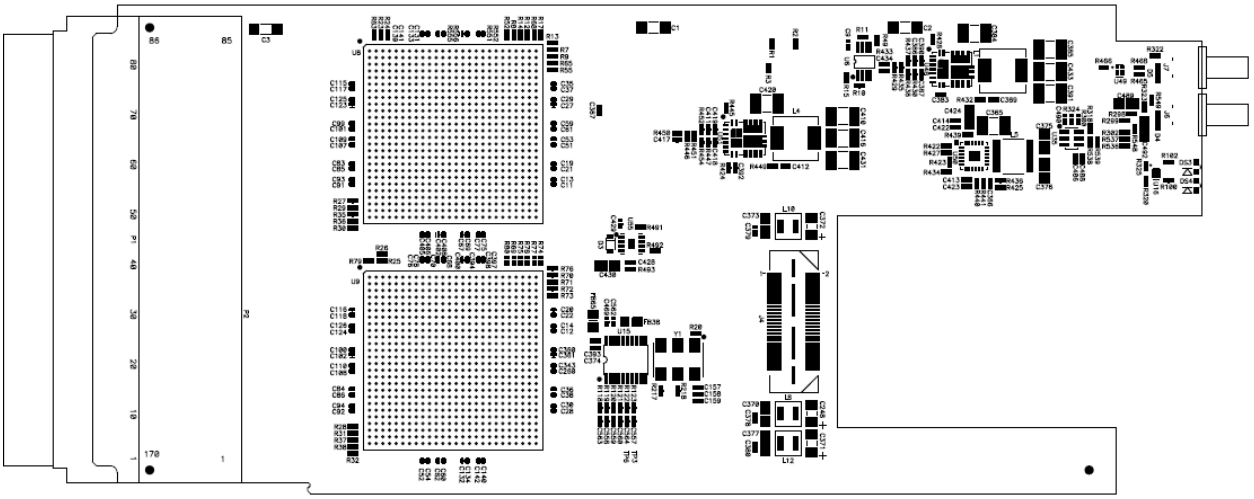

Figure 12: DA118 (SRIO Fabric) component side layout

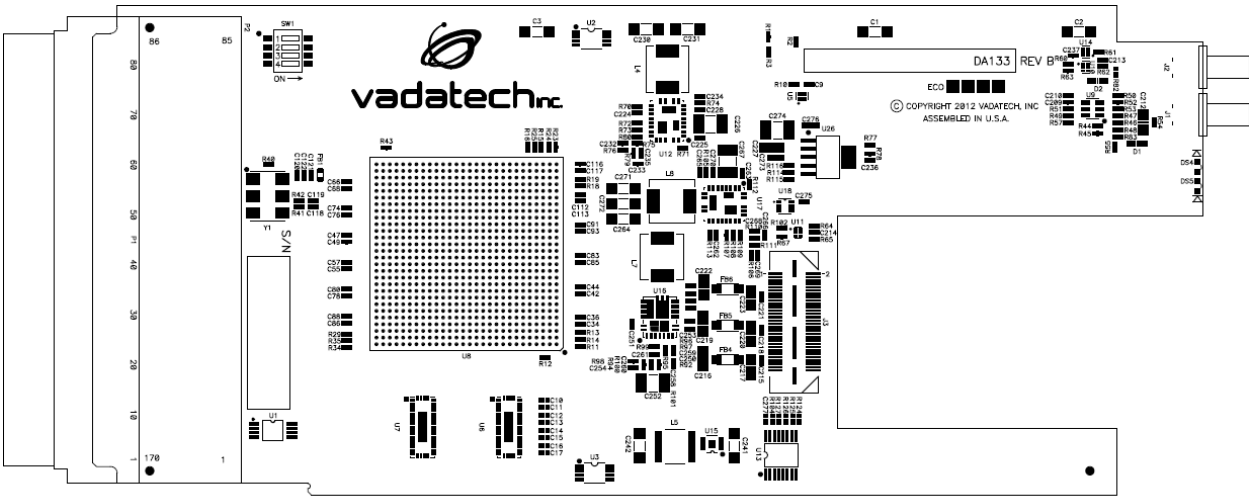

Figure 13: DA133 (SRIO Fabric) component side layout

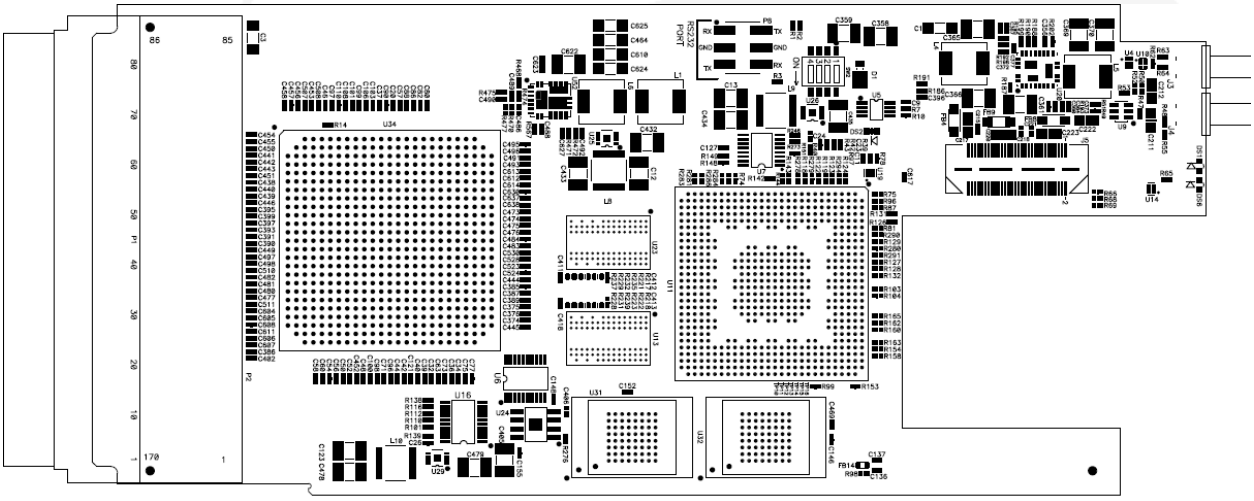

Figure 14: DA134 (CBS Fabric) component side layout

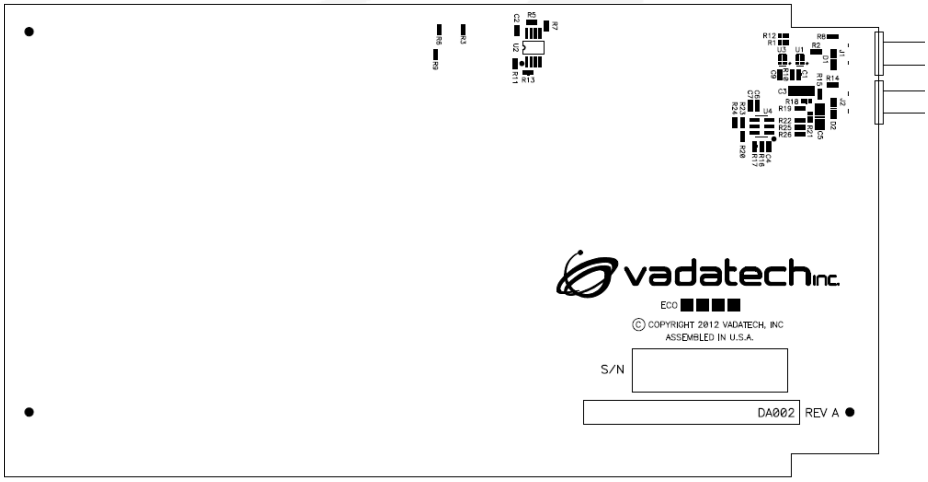

Figure 15: DA002 (Clock I/O Only) component side layout

4 UTC001/UTC002 Architectural Description

A block diagram for the UTC001/UTC002 base board and VT002 daughter card is shown below. Differences between the UTC001 and UTC001 are indicated.

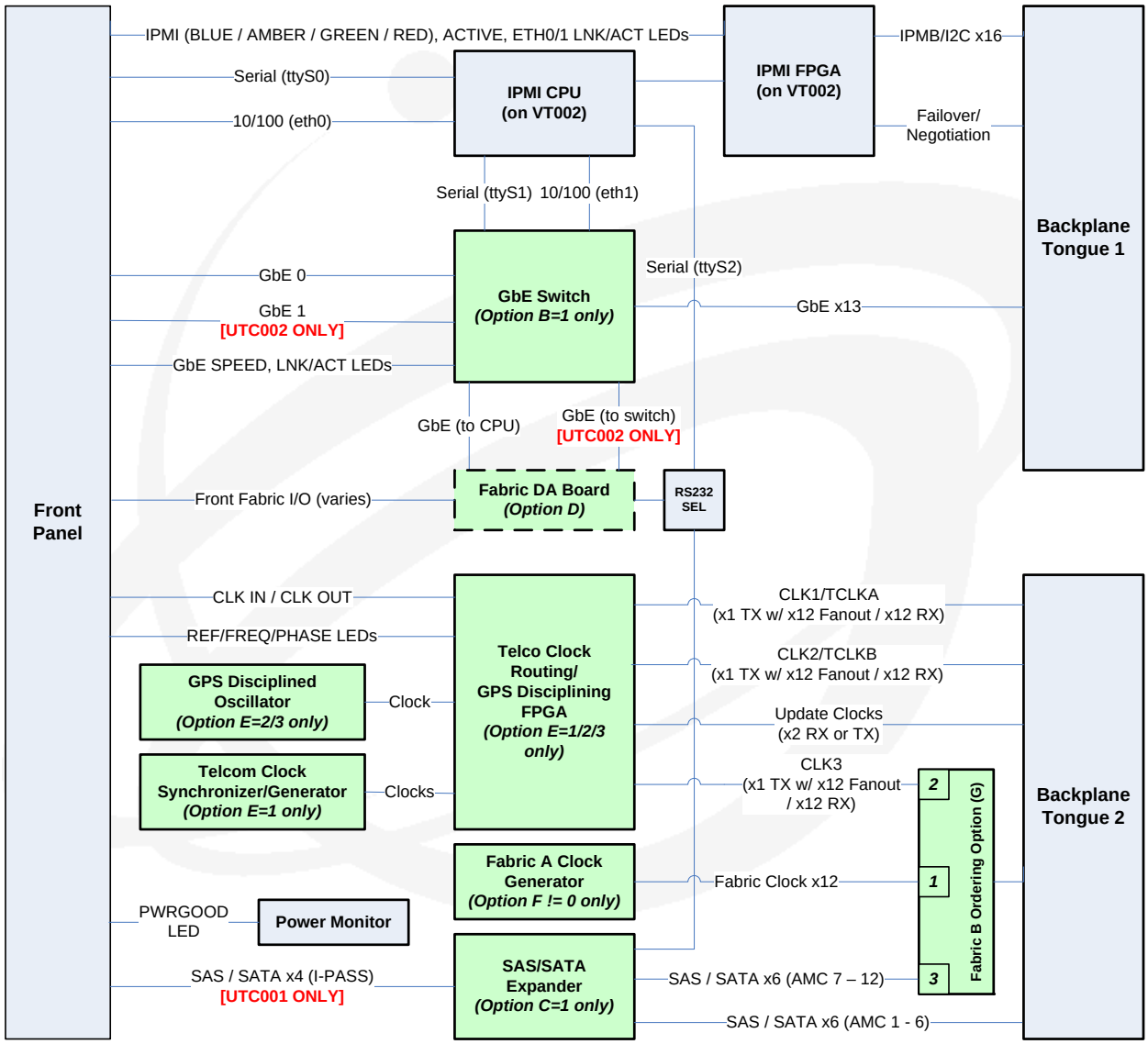

Figure 16: UTC001/UTC002 base block diagram

4.1 IPMI Controller

At its core, the UTC001/UTC002 module contains an IPMI Controller (VT002 board) made up of a 400 MHz CPU and custom FPGA for carrier/shelf management. This controller includes separate IPMB buses for Host, Local, IPMB-A, IPMB-B, CF-A, CF-B, and up to 12 AMC slots. Each IPMB bus has an associated 128-byte RX FIFO and 128-byte TX FIFO to provide improved parallelism and performance using CPU interrupt coalescing. The controller includes an integrated activation/failover arbiter at the hardware level for seamless failover between two UTC001 or UTC002 modules. The IPMI Controller provides a serial port on the front panel for gaining access to the Linux OS console. It also provides a 10/100 Ethernet port (eth0) to the front panel for out-of-band access and internally has a 10/100 Ethernet port (eth1) to the 1GbE switch for in-band access.

Further details on the IPMI controller can be found in the VadaTech MicroTCA MCH Getting Started Guide (& related software documents).

4.2 1GbE Layer 2 Managed Switch Option (B = 1)

An optional 1GbE switch is provided which includes an integrated 266 MHz CPU providing Layer 2 management. This switch connects to up to 12 AMC slots, one front panel RJ45 on the UTC001 (GbE) or two front panel ports on the UTC002 (GbE 0/1), the VT002 internal port (eth1), a connection to the DA112/DA116 10GbE management CPU plus (only on the UTC002) a direct link to the 10GbE switch fabric, and also has an update channel link to the second UTC001/UTC002 when present. A serial port connection is present between the switch management CPU and the IPMI Controller CPU. However, the primary management for this switch is via a supplied web interface. Please do not use the serial port connection unless instructed by VadaTech.

The port configuration of the 1GbE switch is as follows for the UTC001 and then the UTC002:

Logical Port #	Port Description	Logical Port #	Port Description
1	AMC 1	9	AMC 9
2	AMC 2	10	AMC 10
3	AMC 3	11	AMC 11
4	AMC 4	12	AMC 12
5	AMC 5	13	VT002 IPMI (eth1)
6	AMC 6	14	Front Panel (GbE)
7	AMC 7	15	DA112 10GbE CPU
8	AMC 8	16	MCH <-> MCH

Table 2: UTC001 Port mapping of the 1GBE switch

Logical Port #	Port Description	Logical Port #	Port Description
1	AMC 1	10	AMC 10
2	AMC 2	11	AMC 11
3	AMC 3	12	AMC 12
4	AMC 4	13	VT002 IPMI (eth1)
5	AMC 5	14	MCH <-> MCH
6	AMC 6	15	DA116 10GbE CPU
7	AMC 7	16	DA116 10GbE Switch
8	AMC 8	17	Front Panel (GbE 0)
9	AMC 9	18	Front Panel (GbE 1)

Table 3: UTC002 Port mapping of the 1GBE switch

NOTE: On the UTC001 the 1GbE and 10GbE segments can be bridged via the 10GbE switch management CPU, while on the UTC002 these segments can be bridged directly via a dedicated 1GbE link between the two switches. Wire-speed bridging can be expected on the UTC002 but NOT on the UTC001 due to the need for software-based forwarding.

Further details on the 1GbE switch can be found in the VadaTech Gigabit Ethernet Managed Switch Setup Guide and VadaTech Gigabit Ethernet Switch Web Interface Reference Manual.

4.3 SAS/SATA Expander Option (C = 1)

An optional SAS/SATA expander is available which includes an integrated CPU providing SAS management. This expander connects to up to 12 AMC slots (x1 links), a front panel I-PASS connector (x4 wide-link) [UTC001 only], and also has an update channel link (x1 link) to the second UTC001/UTC002 when present. A serial port connection is present between the expander management CPU and the IPMI Controller CPU. Please do not use the serial port connection unless instructed by VadaTech. Ordering option 'G' affects which AMCs the SAS/SATA expander connects to. The following table shows the connectivity for each option:

Option 'G'	Selection Name	SAS/SATA AMC Connectivity
0	None	No AMC connections
1	Fabric clock shared with Fabric B	Connection to AMC Slots 1 – 6 only
2	Telcom clock shared with Fabric B	Connection to AMC Slots 1 – 6 only
3	No clocks – all Fabric B	Connection to all AMC Slots 1 – 12

Table 4: SAS/SATA connectivity options

The port configuration for the SAS/SATA Expander is as follows:

Physical Port #	Port Description	Physical Port #	Port Description
0	AMC 1	9	AMC 10
1	AMC 2	10	AMC 11
2	AMC 3	11	AMC 12
3	AMC 4	12	MCH <-> MCH
4	AMC 5	13	Front Panel (x4) [UTC001 only]
5	AMC 6	14	
6	AMC 7	15	
7	AMC 8	16	
8	AMC 9	17	Reserved

Table 5: SAS/SATA expander port mapping

4.4 Fabric Clock Option (F = 1)

The base board also includes a 100 MHz PCIe clock generator option. This clock generator provides clocking to up to 12 AMC slots. It can be configured with Spread Spectrum Clocking (SSC) on or off. This centralized fabric clock is required when SSC is desired for the PCIe fabric in the chassis and is strongly recommended for PCIe fabrics even if SSC is not used. Other types of fabric clock are possible; please contact VadaTech sales with your requirement.

Whenever the fabric clock option is selected, you should also select Option 'G' as '1' so that the fabric clock will be visible to the AMC slots. The connectivity for the fabric clock is shown below:

Option 'G'	Selection Name	Fabric Clock Connectivity
0	None	No AMC connections
1	Fabric clock shared with Fabric B	Connection to all AMC Slots 1 – 12
2	Telcom clock shared with Fabric B	No AMC connections
3	No clocks – all Fabric B	No AMC connections

Table 6: Fabric clock connectivity options

4.5 Telcom TCXO Clock Option (E = 1)

The base board includes two different options for Telco clocking. There is an ordering option 'E=1' for Telcom clock synchronization/generation which supports many telecom standards such as T1/E1/SDH with an on-board Stratum 3 oscillator and automatic failover/holdover.

The Telcom synchronizer supports the following input clock frequencies:

2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz, and 19.44 MHz

The Telcom clock generator outputs the following clock frequencies:

1.544 MHz (T1/DS1)
2.048 MHz (E1)
3.088 MHz, 16.384 MHz, and 19.44 MHz (SDH)
4.096 MHz and 8.192 MHz or 32.768 MHz and 65.536 MHz
6.312 MHz (DS2), 8.448 MHz (E2), 44.736 MHz (DS3), or 34.368 MHz (E3)
5 styles of 8 kHz framing pulses
2 kHz multi-frame pulse

The REF, FREQ, and PHASE LEDs are updated based on the Telcom synchronizer status. A complete description of the Telcom/GPS clocking functionality of the UTC001/UTC002 can be found in the VadaTech MicroTCA Telco / GPS Clock Configuration Guide document.

4.6 GPS VCTCXO Clock Option (E = 2, 3, or 5)

The other Telcom clocking option is a GPS disciplined oscillator solution. The GPS disciplined oscillator takes in a 1 Pulse-Per-Second (1PPS) reference from a GPS receiver (sold separately) and disciplines a Stratum 3 10 MHz, 30.72 MHz, or 50MHz oscillator depending on the ordering option and outputs this frequency as well as a regenerated 1PPS signal which is phase aligned to the reference. Automatic holdover mode is activated any time the reference is lost. The regenerated 1PPS pulse continues to be generated even during holdover when the reference pulse would otherwise be missing.

The REF, FREQ, and PHASE LEDs are updated based on the GPS disciplining algorithm's status. A complete description of the Telcom/GPS clocking functionality of the UTC001 can be found in the UTC001 and VT850 Telco / GPS Clock Configuration Guide document.

4.7 Telco Clock Distribution Support (E != 0)

Both of the Telco and GPS clock ordering options include clock routing support based on the AMC.0 v1 and AMC.0 v2 specifications, and a clock distribution only option E=4 is also available if on-board clock synchronization is not necessary. The clock router can provide M-LVDS clocking signals to up to 12 AMC slots on CLK1/TCLKA, CLK2/TCLKB, or CLK3. It also provides a front panel SMA [UTC001] or SMB [UTC002] clock output, two update channel clock paths to the second UTC001/UTC002 (when present), and internal on-board destinations such as the Telcom clock synchronizer/GPS reference 1PPS. The clock router can be configured to select the sources of these clocks from any of the 12 AMC slots on CLK1/TCLKA, CLK2/TCLKB, or CLK3, from the front panel SMB [UTC001] or SMA [UTC002] clock input, from one of the update clock paths from the second UTC001/UTC002 (when present), or from internal on-board sources such as the Telcom clock generator/GPS oscillator/1PPS.

Note that AMC TCLKC and TCLKD were added in the AMC.0 v2 specification after the uTCA specification was developed and therefore they are not supported by the uTCA MCH pin-out. Therefore these clocks are not supported by the UTC001/UTC002. If you require routing of these clocks please consider the VadaTech VT85x family of 1U chassis or the VadaTech VT864 which include AMC TCLKC and TCLKD routing capability. The ordering option 'G' affects how the CLK3 channels will connect to the AMC slots.

The following table shows the connectivity for each option:

Option 'G'	Selection Name	Telco CLK3 Connectivity (non-fabric usage)
0	None	No AMC connections
1	Fabric clock shared with Fabric B	No AMC connections
2	Telcom clock shared with Fabric B	Connection to all AMC Slots 1 – 12
3	No clocks – all Fabric B	No AMC connections

Table 7: Telco clock connectivity options

A complete description of the Telcom/GPS clocking functionality of the UTC001/UTC002 can be found in the VadaTech MCH Telco / GPS Clock Configuration Guide document.

4.8 No Fabric w/ Clocking I/O Option - DA002 (UTC002 E != 0)

The DA002 provides no fabric connection to the backplane MCH tongues 3 and 4. It only provides front clocking capability which is compatible with the front clocking capability provided on the other UTC002 fabric daughter cards.

Please refer to the VadaTech MCH Telco / GPS Clock Configuration Guide document for further details regarding clocking I/O for all MCH variations.

4.9 PCIe Fabric Option – DA111 (UTC001 D = 1)

The DA111 daughter card provides a PCIe Gen2 (5 GT/s) x4 switching fabric on MCH Tongues 3 and 4. The PCIe switch has connections to up to 12 AMCs (x4 wide links with automatic x1 downshift) and a front panel I-PASS (x4 wide link) for chassis-to-chassis or PC-to-chassis expansion. The switch will automatically downshift to Gen1 (2.5 GT/s) on a port-by-port basis depending on what is connected. The upstream (host) port is determined by E-Keying, and the AMC with this port is activated last so that all of the downstream devices are present prior to the host seeing the PCIe fabric.

NOTE: When selecting the PCIe fabric option (D=1) you must also select the Fabric Clock option (F=1) since this is needed for the PCIe fabric operation. Also to enable Spread Spectrum Clocking (SSC) and to maximize AMC compatibility it is strongly recommended that you also select the Fabric B ports Configuration option of G=1 [Fabric clock shared with Fabric B (SAS)] as this will ensure that the PCIe clock goes to all AMCs and they can properly synchronize with the fabric. If option G is not selected as 1 then SSC **cannot** be used. Furthermore, even if SSC is not used there may still be compatibility problems with AMCs which are designed to expect a fabric clock to be provided by the MCH. Therefore, for PCIe fabric VadaTech recommends the option combination of D=1, F=1, G=1.

The port configuration of the PCIe switch is as follows:

Physical Port #	Port Description	Physical Port #	Port Description
0 – 3	AMC 1 (x4)	24 – 27	AMC 7 (x4)
4 – 7	AMC 2 or Front I-PASS (x4)	28 – 31	AMC 8 (x4)
8 – 11	AMC 3 (x4)	32 – 35	AMC 9 (x4)
12 – 15	AMC 4 (x4)	36 – 39	AMC 10 (x4)
16 – 19	AMC 5 (x4)	40 – 43	AMC 11 (x4)
20 - 23	AMC 6 (x4)	44 - 47	AMC 12 (x4)

Table 8: PCIe configuration

NOTE: When the front panel connector is selected for use, AMC slot 2 will not be connected to the fabric due to port sharing on the switch. This selection is made by software.

4.10 10GbE Fabric Option – DA112 (UTC001 D = 3 or 4)

The DA112 daughter card provides a 10GbE (XAUI) switching fabric on MCH Tongues 3 and 4. The DA112 includes an on-board 400 MHz management CPU which runs a Layer 2 switch management stack. Ordering option 'D' must be '4' (light managed) or if ordering option '3' is used, the result is still the same behavior as '4'. The 10GbE switch connects to up to 12 AMC slots (XAUI), a front panel I-PASS connector (XAUI), the on-board management CPU (1GbE – eth0), and an update channel link (XAUI) to the second UTC001 when present. The management CPU also has a 1GbE (eth1) connection to the 1GbE switch on the base board.

On the UTC001, routing or bridging is possible between the 10GbE segment and the 1GbE segment via the switch management CPU. The same capability exists on the UTC002 but there is also a dedicated link between the 1GbE and 10GbE switches on this module which usually is preferable. Line rate bridging can be expected on the UTC002 but NOT on the UTC001 due to the use of software-based bridging.

The following block diagram shows the DA112 (UTC001) architecture:

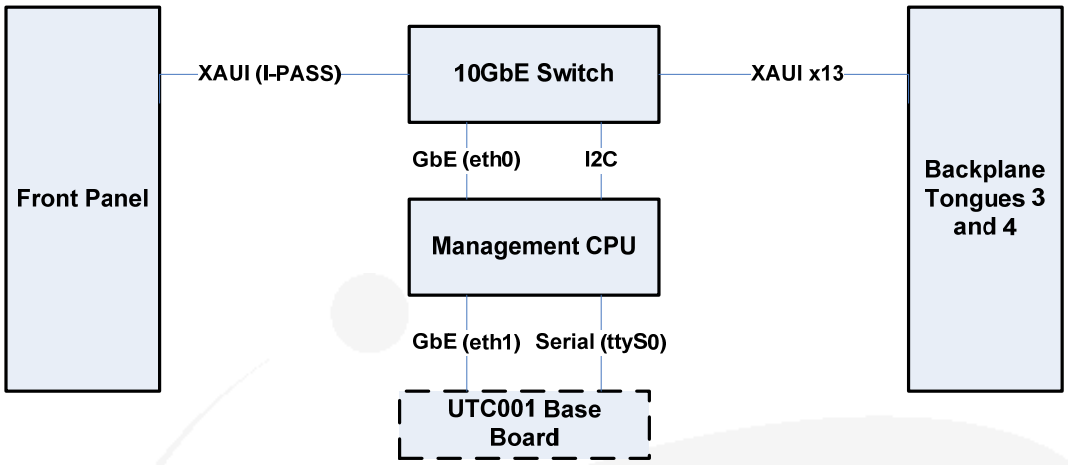

Figure 17: DA112 (UTC001) block diagram

The following table shows the port mapping of the DA112:

Physical Port #	Port Description	Physical Port #	Port Description
0	AMC 3 (XAUI)	10	(no connect)
1	(no connect)	11	AMC 8 (XAUI)
2	(no connect)	12	AMC 11 (XAUI)
3	AMC 9 (XAUI)	13	AMC 6 (XAUI)
4	AMC 10 (XAUI)	14	Front I-PASS (XAUI)
5	(no connect)	15	AMC 1 (XAUI)
6	(no connect)	16	AMC 5 (XAUI)
7	AMC 2 (XAUI)	17	AMC 12 (XAUI)
8	AMC 4 (XAUI)	18	MCH <-> MCH (XAUI)
9	Management CPU (1GbE – eth0)	19	AMC 7 (XAUI)

Table 9: DA112 (UTC001) 10GBE switch port mapping

4.11 SRIO Fabric Option - DA113 (UTC001 D = 2)

The DA113 daughter card provides SRIO x4 switching fabric on MCH Tongues 3 and 4. Ordering option 'D' must be '2' to receive this functionality. The SRIO switch connects to up to 12 AMCs (x4) as well as a front I-PASS (x4) connector for expansion. The SRIO fabric is made up of two on-board switches, one of which handles AMC slots 1-6 and other of which handles slots 7-12 and the front port. The two switches are cross-connected using three x4 links.

The port configuration of the two switches is shown below:

Switch #	Physical Port #	Port Description
0	0 – 3	AMC 6 (x4)
0	4 – 7	AMC 5 (x4)
0	8 – 11	AMC 4 (x4)
0	12 – 15, 20 - 23, 28 - 31	SWITCH <-> SWITCH (3 x4)
0	16 – 19	AMC 1 (x4)
0	24 – 27	AMC 3 (x4)
0	32 – 35	Front I-PASS (x4)
0	36 – 39	AMC 2 (x4)
1	0 – 3	AMC 10 (x4)
1	4 – 7	AMC 9 (x4)
1	8 – 11	AMC 8 (x4)
1	12 – 15	AMC 7 (x4)
1	16 – 19	AMC 11 (x4)
1	20 – 23, 28 – 35	SWITCH <-> SWITCH (3 x4)
1	24 – 27	Update (MCH <-> MCH x4)
1	36 – 39	AMC 12 (x4)

Table 10: SRIO x4 switching fabric port configuration

4.12 PCIe Fabric Option – DA115 (UTC001 D=5)

The DA115 daughter card provides a PCIe Gen2 (5.0 GT/s) x4 switching fabric with partitioning on MCH Tongues 3 and 4. The PCIe switch has connections to up to 12 AMCs (x4 wide links with automatic x1 downshift) and a front panel I-PASS (x4 wide link) for chassis-to-chassis or PC-to-chassis expansion. The switch will automatically downshift to Gen1 (2.5 GT/s) on a port-by-port basis depending on what is connected. The upstream (host) port is determined by E-Keying, and the AMC with this port is activated last so that all of the downstream devices are present prior to the host seeing the PCIe fabric.

NOTE: When selecting the PCIe fabric option (D=5) you must also select the Fabric Clock option (F=1) since this is needed for the PCIe fabric operation. Also to enable Spread Spectrum Clocking (SSC) and to maximize AMC compatibility it is strongly recommended that you also select the Fabric B ports Configuration option of G=1 [Fabric clock shared with Fabric B (SAS)] as this will ensure that the PCIe clock goes to all AMCs and they can properly synchronize with the fabric. If option G is not selected as 1 then SSC **cannot** be used. Furthermore, even if SSC is not used there may still be compatibility problems with AMCs which are designed to expect a fabric clock to be provided by the MCH. Therefore, for PCIe fabric with partitioning VadaTech recommends the option combination of D=5, F=1, G=1.

The port configuration of the PCIe switch is as follows:

Physical Port #	Port Description	Physical Port #	Port Description
0 – 3	AMC 8 (x4)	24 – 27	AMC 4 (x4)
4 – 7	AMC 2 (x4)	28 – 31	AMC 10 (x4)
8 – 11	AMC 1 (x4)	32 – 35	AMC 12 or Front I-PASS (x4)
12 – 15	AMC 7 (x4)	36 – 39	AMC 6 (x4)
16 – 19	AMC 9 (x4)	40 – 43	AMC 5 (x4)
20 - 23	AMC 3 (x4)	44 - 47	AMC 11 (x4)

Table 11: PCIe configuration

NOTE: When the front panel connector is selected for use, AMC slot 12 will not be connected to the fabric due to port sharing on the switch. This selection is made by software.

The switch partitioning (multi-root complex support) is configured via software.

4.13 10GbE Fabric Option – DA116 (UTC002 D = 3 or 4)

The DA116 daughter card provides a 10GbE (XAUI) switching fabric on MCH Tongues 3 and 4. The DA116 includes an on-board 400 MHz management CPU which runs a Layer 2 switch management stack. Ordering option 'D' must be '4' (light managed) or if ordering option '3' is used, the result is still the same behavior as '4'. The 10GbE switch connects to up to 12 AMC slots (XAUI), two SFP+ modules on the front, the on-board management CPU (1GbE – eth0), the 1GbE switch on the base-board, and an update channel link (XAUI) to the second UTC002 when present. The management CPU also has a 1GbE (eth1) connection to the 1GbE switch on the base board.

On the UTC001, routing or bridging is possible between the 10GbE segment and the 1GbE segment via the switch management CPU. The same capability exists on the UTC002 but there is also a dedicated link between the 1GbE and 10GbE switches on this module which usually is preferable. Line rate bridging can be expected on the UTC002 but NOT on the UTC001 due to the use of software-based bridging.

The following block diagram shows the DA116 (UTC002) architecture:

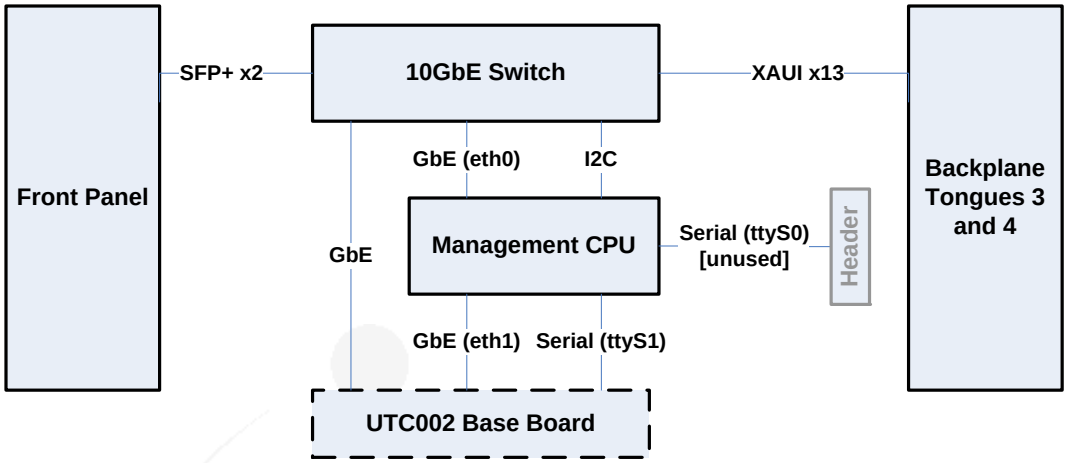

Figure 18: DA116 (UTC002) block diagram

The following table shows the port mapping of the DA116:

Physical Port #	Port Description	Physical Port #	Port Description
0	AMC 3 (XAUI/1GbE)	10	Front SFP+ 1 (10GbE/1GbE auto SFP detect)
1	1G Switch-to-10G switch (1GbE)	11	AMC 8 (XAUI/1GbE)
2	(no connect)	12	AMC 11 (XAUI/1GbE)
3	AMC 9 (XAUI/1GbE)	13	AMC 6 (XAUI/1GbE)
4	AMC 10 (XAUI/1GbE)	14	Front SFP+ 0 (10GbE/1GbE auto SFP detect)
5	(no connect)	15	AMC 1 (XAUI/1GbE)
6	(no connect)	16	AMC 5 (XAUI/1GbE)
7	AMC 2 (XAUI/1GbE)	17	AMC 12 (XAUI/1GbE)
8	AMC 4 (XAUI/1GbE)	18	MCH <-> MCH (XAUI/1GbE)
9	Management CPU (1GbE – eth0)	19	AMC 7 (XAUI/1GbE)

Table 12: DA116 (UTC002) 10GBE switch port mapping

4.14 PCIe Fabric Option – DA117 (UTC002 D=5)

The DA115 daughter card provides a PCIe Gen2 (5.0 GT/s) x4 switching fabric with partitioning on MCH Tongues 3 and 4. The PCIe switch has connections to up to 12 AMCs (x4 wide links with automatic x1 downshift) and a front panel QSFP (x4 wide link) for chassis-to-chassis or PC-to-chassis expansion. The switch will automatically downshift to Gen1 (2.5 GT/s) on a port-by-port basis depending on what is connected. The upstream (host) port is determined by E-Keying, and the AMC with this port is activated last so that all of the downstream devices are present prior to the host seeing the PCIe fabric.

NOTE: When selecting the PCIe fabric option (D=5) you must also select the Fabric Clock option (F=1) since this is needed for the PCIe fabric operation. Also to enable Spread Spectrum Clocking (SSC) and to maximize AMC compatibility it is strongly recommended that you also select the Fabric B ports Configuration option of G=1 [Fabric clock shared with Fabric B (SAS)] as this will ensure that the PCIe clock goes to all AMCs and they can properly synchronize with the fabric. If option G is not selected as 1 then SSC **cannot** be used. Furthermore, even if SSC is not used there may still be compatibility problems with AMCs which are designed to expect a fabric clock to be provided by the MCH. Therefore, for PCIe fabric with partitioning VadaTech recommends the option combination of D=5, F=1, G=1.

The port configuration of the PCIe switch is as follows:

Physical Port #	Port Description	Physical Port #	Port Description
0 – 3	AMC 8 (x4)	24 – 27	AMC 4 (x4)
4 – 7	AMC 11 (x4)	28 – 31	AMC 10 (x4)
8 – 11	AMC 1 (x4)	32 – 35	AMC 12 or Front I-PASS (x4)
12 – 15	AMC 7 (x4)	36 – 39	AMC 6 (x4)
16 – 19	AMC 9 (x4)	40 – 43	AMC 5 (x4)
20 - 23	AMC 3 (x4)	44 - 47	AMC 2 (x4)

Table 13: PCIe configuration

NOTE: When the front panel connector is selected for use, AMC slot 12 will not be connected to the fabric due to port sharing on the switch. This selection is made by software.

The switch partitioning (multi-root complex support) is configured via software.

4.15 SRIO Fabric Option - DA118 (UTC002 D = 2)

The DA118 daughter card provides SRIO x4 switching fabric on MCH Tongues 3 and 4. Ordering option 'D' must be '2' to receive this functionality. The SRIO switch connects to up to 12 AMCs (x4) as well as a front QSFP (x4) connector for expansion. The SRIO fabric is made up of two on-board switches, one of which handles AMC slots 1-6 and other of which handles slots 7-12 and the front port. The two switches are cross-connected using three x4 links.

The port configuration of the two switches is shown below:

Switch #	Physical Port #	Port Description
0	0 – 3	AMC 6 (x4)
0	4 – 7	AMC 5 (x4)
0	8 – 11	AMC 4 (x4)
0	12 – 15, 20 - 23, 28 - 31	SWITCH <-> SWITCH (3 x4)
0	16 – 19	AMC 1 (x4)
0	24 – 27	AMC 3 (x4)
0	32 – 35	Front QSFP (x4)
0	36 – 39	AMC 2 (x4)
1	0 – 3	AMC 10 (x4)
1	4 – 7	AMC 9 (x4)
1	8 – 11	AMC 8 (x4)
1	12 – 15	AMC 7 (x4)
1	16 – 19	AMC 11 (x4)
1	20 – 23, 28 – 35	SWITCH <-> SWITCH (3 x4)
1	24 – 27	Update (MCH <-> MCH x4)
1	36 – 39	AMC 12 (x4)

Table 14: SRIO x4 switching fabric port configuration

4.16 CBS Fabric Option - DA132 (UTC001 D = 6)

The DA132 daughter card provides an asynchronous (up to 6.5 Gbps) Cross-Bar Switch (CBS) x4 fabric on MCH Tongues 3 and 4. Ordering option 'D' must be '6' to receive this functionality. The CBS switch connects to up to 12 AMCs (x4) as well as a front I-PASS (x4) connector for expansion. The CBS provides 'circuit-switched' configuration for SERDES lanes, it does NOT 'packet-switch' like other fabrics. This enables static point-to-point or point-to-multipoint SERDES connections to be made between AMCs. The CBS supports fan-out applications (one incoming data stream replicated to multiple outgoing destinations) but does not support fan-in applications (more than one incoming data stream being merged to the same destination).

Note that each input/output lane is uniquely switched. So although four lanes are routed to each AMC, the four lanes can be connected independently. For example rather than carrying one protocol on all four lanes from one source they could carry multiple protocols from the same or different sources by splitting up the lane allocations (i.e. x4, x2+x2, x3+x1, x1+x1+x1+x1, etc). Each output lane can only carry the bit stream from one input lane as if a simple wire were connected from the input to the output. The switch routing configuration is managed by software. By default the ports are grouped into x4 groupings in the configuration file for convenience.

The input and output port configurations of the CBS are shown on the following pages. Note that in these tables the lanes for each port are numbered 0-3. However, these will correspond to either AMC lanes 4-7 or 8-11 depending on which MCH slot the UTC001 is in.

The following block diagram shows the DA132 (UTC001) architecture:

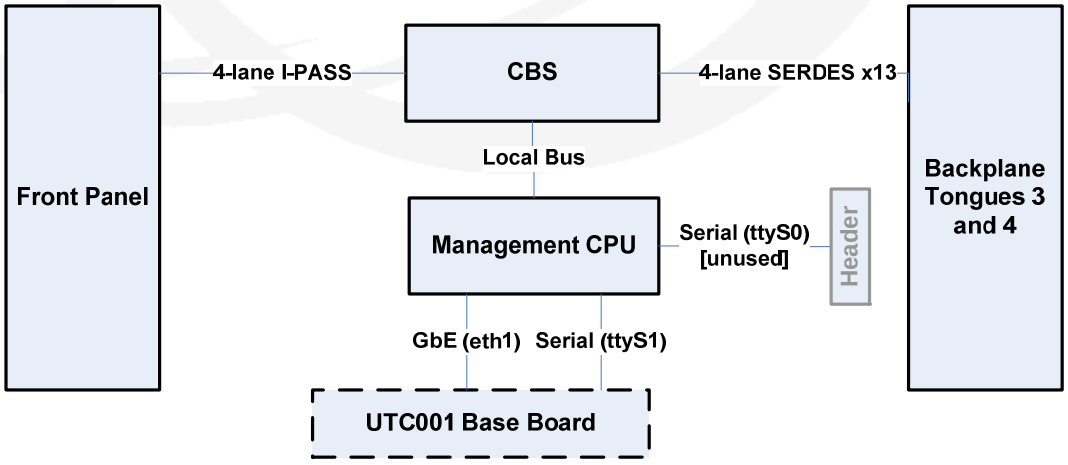

Figure 19: DA132 (UTC001) block diagram

Physical Port A#	Port Description	Physical Port A#	Port Description
0	AMC 12 lane 0	36	n/c
1	Front I-PASS lane 0	37	n/c
2	AMC 12 lane 1	38	AMC 10 lane 0
3	Front I-PASS lane 1	39	AMC 7 lane 1
4	AMC 12 lane 2	40	AMC 10 lane 1
5	Front I-PASS lane 2	41	n/c
6	AMC 12 lane 3	42	AMC 10 lane 2
7	Front I-PASS lane 3	43	AMC 7 lane 2
8	n/c	44	AMC 10 lane 3
9	AMC 1 lane 0	45	AMC 8 lane 3
10	n/c	46	AMC 11 lane 3
11	AMC 1 lane 1	47	AMC 7 lane 3
12	n/c	48	AMC 11 lane 2
13	AMC 1 lane 2	49	AMC 4 lane 0
14	n/c	50	AMC 11 lane 1
15	AMC 1 lane 3	51	AMC 8 lane 2
16	n/c	52	AMC 11 lane 0
17	AMC 2 lane 0	53	AMC 4 lane 1
18	AMC 6 lane 0	54	n/c
19	Update lane 0 (MCH<->MCH)	55	AMC 8 lane 0
20	AMC 6 lane 1	56	AMC 9 lane 3
21	AMC 2 lane 1	57	AMC 4 lane 2
22	AMC 6 lane 2	58	AMC 9 lane 2
23	Update lane 1 (MCH<->MCH)	59	AMC 8 lane 1
24	AMC 6 lane 3	60	AMC 5 lane 0
25	AMC 2 lane 2	61	AMC 4 lane 3
26	n/c	62	AMC 9 lane 1
27	Update lane 2 (MCH<->MCH)	63	AMC 3 lane 0
28	n/c	64	AMC 5 lane 1
29	AMC 2 lane 3	65	AMC 3 lane 1
30	n/c	66	AMC 9 lane 0
31	Update lane 3 (MCH<->MCH)	67	AMC 3 lane 2
32	n/c	68	AMC 5 lane 2
33	n/c	69	AMC 3 lane 3
34	n/c	70	AMC 5 lane 3
35	AMC 7 lane 0	71	n/c

Table 15: CBS x4 switching fabric input port configuration

Physical Port Y#	Port Description	Physical Port Y#	Port Description
0	AMC 12 lane 0	36	n/c
1	AMC 6 lane 0	37	AMC 3 lane 0
2	AMC 12 lane 1	38	n/c
3	AMC 6 lane 1	39	AMC 3 lane 1
4	AMC 12 lane 2	40	n/c
5	AMC 6 lane 2	41	AMC 3 lane 2
6	AMC 12 lane 3	42	n/c
7	AMC 6 lane 3	43	AMC 3 lane 3
8	n/c	44	n/c
9	AMC 4 lane 0	45	AMC 1 lane 0
10	n/c	46	Update lane 3 (MCH<->MCH)
11	AMC 4 lane 1	47	AMC 1 lane 1
12	n/c	48	Update lane 2 (MCH<->MCH)
13	AMC 4 lane 2	49	AMC 1 lane 2
14	n/c	50	Update lane 1 (MCH<->MCH)
15	AMC 4 lane 3	51	AMC 1 lane 3
16	n/c	52	Update lane 0 (MCH<->MCH)
17	AMC 5 lane 0	53	AMC 2 lane 0
18	AMC 10 lane 0	54	Front I-PASS lane 0
19	AMC 5 lane 1	55	AMC 2 lane 1
20	AMC 10 lane 1	56	Front I-PASS lane 1
21	AMC 5 lane 2	57	AMC 2 lane 2
22	AMC 10 lane 2	58	Front I-PASS lane 2
23	AMC 5 lane 3	59	AMC 2 lane 3
24	AMC 10 lane 3	60	Front I-PASS lane 3
25	AMC 9 lane 0	61	AMC 8 lane 0
26	n/c	62	n/c
27	AMC 9 lane 1	63	AMC 8 lane 1
28	AMC 11 lane 0	64	AMC 7 lane 0
29	AMC 9 lane 2	65	AMC 8 lane 2
30	AMC 11 lane 1	66	AMC 7 lane 1
31	AMC 9 lane 3	67	AMC 8 lane 3
32	AMC 11 lane 2	68	AMC 7 lane 2
33	n/c	69	n/c
34	AMC 11 lane 3	70	AMC 7 lane 3
35	n/c	71	n/c

Table 16: CBS x4 switching fabric output port configuration

4.17 SRIO Fabric Option – DA133 (UTC002 D=7)

The DA133 daughter card provides SRIO Gen 2 x4 switching fabric on MCH Tongues 3 and 4. Ordering option 'D' must be '7' to receive this functionality. The SRIO switch connects to up to 12 AMCs (x4) as well as a front QSFP (x4) connector for expansion.

The port configuration of the switch is shown below:

Physical Port #	Port Description
0 – 3	AMC 3 (x4)
4 – 7	AMC 6 (x4)
8 – 11	AMC 9 (x4)
12 – 15	AMC 11 (x4)
16 – 19	AMC 1 (x4)
20 – 23	AMC 4 (x4)
24 – 27	AMC 7 (x4)
28 - 31	AMC 12 or Front QSFP (x4)
32 – 35	AMC 2 (x4)
36 – 39	AMC 5 (x4)
40 – 43	AMC 8 (x4)
44 – 47	AMC 10 (x4)

Table 17: SRIO x4 switching fabric port configuration

NOTE: When the front expansion port is used, AMC 12 is disconnected from the fabric due to port sharing. Port routing is configured by software.

4.18 CBS Fabric Option - DA134 (UTC002 D = 6)

The DA134 daughter card provides an asynchronous (up to 6.5 Gbps) Cross-Bar Switch (CBS) x4 fabric on MCH Tongues 3 and 4. Ordering option 'D' must be '6' to receive this functionality. The CBS switch connects to up to 12 AMCs (x4) as well as a front QSFP (x4) connector for expansion. The CBS provides 'circuit-switched' configuration for SERDES lanes, it does NOT 'packet-switch' like other fabrics. This enables static point-to-point or point-to-multipoint SERDES connections to be made between AMCs. The CBS supports fan-out applications (one incoming data stream replicated to multiple outgoing destinations) but does not support fan-in applications (more than one incoming data stream being merged to the same destination).

Note that each input/output lane is uniquely switched. So although four lanes are routed to each AMC, the four lanes can be connected independently. For example rather than carrying one protocol on all four lanes from one source they could carry multiple protocols from the same or different sources by splitting up the lane allocations (i.e. x4, x2+x2, x3+x1, x1+x1+x1+x1, etc). Each output lane can only carry the bit stream from one input lane as if a simple wire were connected from the input to the output. The switch routing configuration is managed by software. By default the ports are grouped into x4 groupings in the configuration file for convenience.

The input and output port configurations of the CBS are shown on the following pages. Note that in these tables the lanes for each port are numbered 0-3. However, these will correspond to either AMC lanes 4-7 or 8-11 depending on which MCH slot the UTC002 is in.

The following block diagram shows the DA134 (UTC002) architecture:

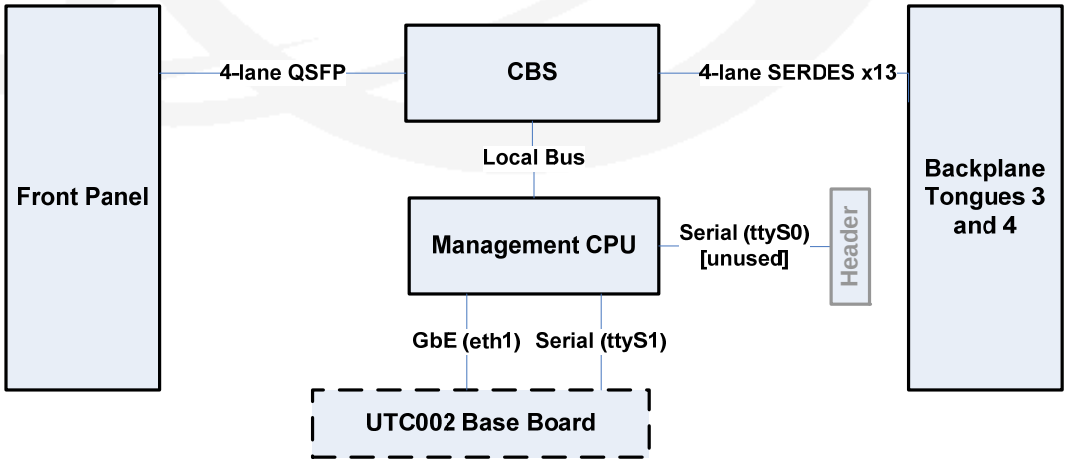

Figure 20: DA132 (UTC001) block diagram

Physical Port A#	Port Description	Physical Port A#	Port Description
0	AMC 12 lane 0	36	n/c
1	Front I-PASS lane 0	37	n/c
2	AMC 12 lane 1	38	AMC 10 lane 0
3	Front I-PASS lane 1	39	AMC 7 lane 1
4	AMC 12 lane 2	40	AMC 10 lane 1
5	Front I-PASS lane 2	41	n/c
6	AMC 12 lane 3	42	AMC 10 lane 2
7	Front I-PASS lane 3	43	AMC 7 lane 2
8	n/c	44	AMC 10 lane 3
9	AMC 1 lane 0	45	AMC 8 lane 3
10	n/c	46	AMC 11 lane 3
11	AMC 1 lane 1	47	AMC 7 lane 3
12	n/c	48	AMC 11 lane 2
13	AMC 1 lane 2	49	AMC 4 lane 0
14	n/c	50	AMC 11 lane 1
15	AMC 1 lane 3	51	AMC 8 lane 2
16	n/c	52	AMC 11 lane 0
17	AMC 2 lane 0	53	AMC 4 lane 1
18	AMC 6 lane 0	54	n/c
19	Update lane 0 (MCH<->MCH)	55	AMC 8 lane 0
20	AMC 6 lane 1	56	AMC 9 lane 3
21	AMC 2 lane 1	57	AMC 4 lane 2
22	AMC 6 lane 2	58	AMC 9 lane 2
23	Update lane 1 (MCH<->MCH)	59	AMC 8 lane 1
24	AMC 6 lane 3	60	AMC 5 lane 0
25	AMC 2 lane 2	61	AMC 4 lane 3
26	n/c	62	AMC 9 lane 1
27	Update lane 2 (MCH<->MCH)	63	AMC 3 lane 0
28	n/c	64	AMC 5 lane 1
29	AMC 2 lane 3	65	AMC 3 lane 1
30	n/c	66	AMC 9 lane 0
31	Update lane 3 (MCH<->MCH)	67	AMC 3 lane 2
32	n/c	68	AMC 5 lane 2
33	n/c	69	AMC 3 lane 3
34	n/c	70	AMC 5 lane 3
35	AMC 7 lane 0	71	n/c

Table 18: CBS x4 switching fabric input port configuration

Physical Port Y#	Port Description	Physical Port Y#	Port Description
0	AMC 12 lane 0	36	n/c
1	AMC 6 lane 0	37	AMC 3 lane 0
2	AMC 12 lane 1	38	n/c
3	AMC 6 lane 1	39	AMC 3 lane 1
4	AMC 12 lane 2	40	n/c
5	AMC 6 lane 2	41	AMC 3 lane 2
6	AMC 12 lane 3	42	n/c
7	AMC 6 lane 3	43	AMC 3 lane 3
8	n/c	44	n/c
9	AMC 4 lane 0	45	AMC 1 lane 0
10	n/c	46	Update lane 3 (MCH<->MCH)
11	AMC 4 lane 1	47	AMC 1 lane 1
12	n/c	48	Update lane 2 (MCH<->MCH)
13	AMC 4 lane 2	49	AMC 1 lane 2
14	n/c	50	Update lane 1 (MCH<->MCH)
15	AMC 4 lane 3	51	AMC 1 lane 3
16	n/c	52	Update lane 0 (MCH<->MCH)
17	AMC 5 lane 0	53	AMC 2 lane 0
18	AMC 10 lane 0	54	Front I-PASS lane 0
19	AMC 5 lane 1	55	AMC 2 lane 1
20	AMC 10 lane 1	56	Front I-PASS lane 1
21	AMC 5 lane 2	57	AMC 2 lane 2
22	AMC 10 lane 2	58	Front I-PASS lane 2
23	AMC 5 lane 3	59	AMC 2 lane 3
24	AMC 10 lane 3	60	Front I-PASS lane 3
25	AMC 9 lane 0	61	AMC 8 lane 0
26	n/c	62	n/c
27	AMC 9 lane 1	63	AMC 8 lane 1
28	AMC 11 lane 0	64	AMC 7 lane 0
29	AMC 9 lane 2	65	AMC 8 lane 2
30	AMC 11 lane 1	66	AMC 7 lane 1
31	AMC 9 lane 3	67	AMC 8 lane 3
32	AMC 11 lane 2	68	AMC 7 lane 2
33	n/c	69	n/c
34	AMC 11 lane 3	70	AMC 7 lane 3
35	n/c	71	n/c

Table 19: CBS x4 switching fabric output port configuration

4.19 UTC001 Front Panel

The conceptual front panel of the UTC001 shown below consists of the MCH hot-swap handle, IPMI LEDs, RJ45 for IPMI Serial Console port, RJ45 for IPMI 10/100 Ethernet port, RJ-45 for the GbE Switch, I-PASS for SAS/SATA expansion, I-PASS for PCIe or SRIO or 10GbE expansion, SMA clock in/out for Telcom clocking, and various status LEDs. The figures below show the front panel connections with callouts to help clarify the purpose of connectors/LEDs:

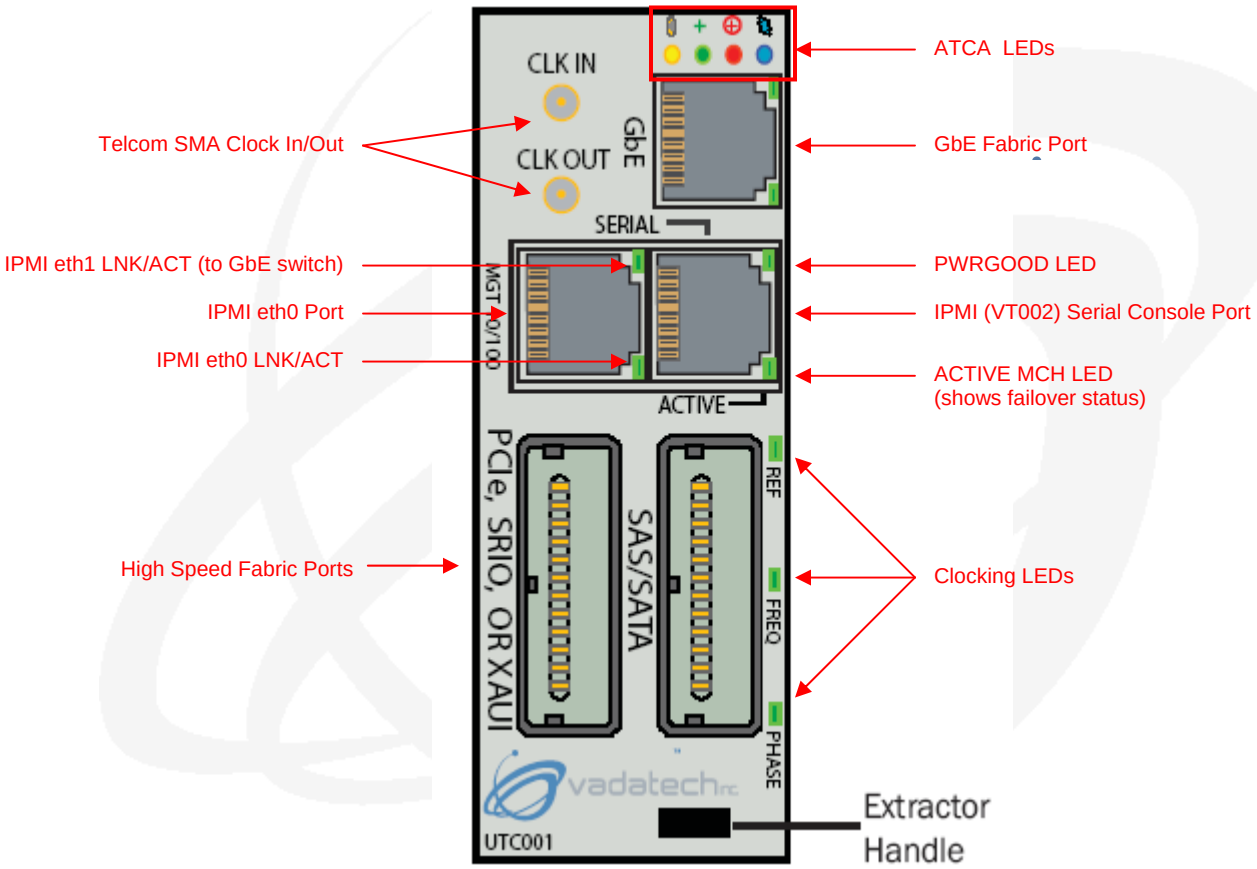

Figure 21: UTC001 front panel

4.20 UTC001 Front Panel Variations

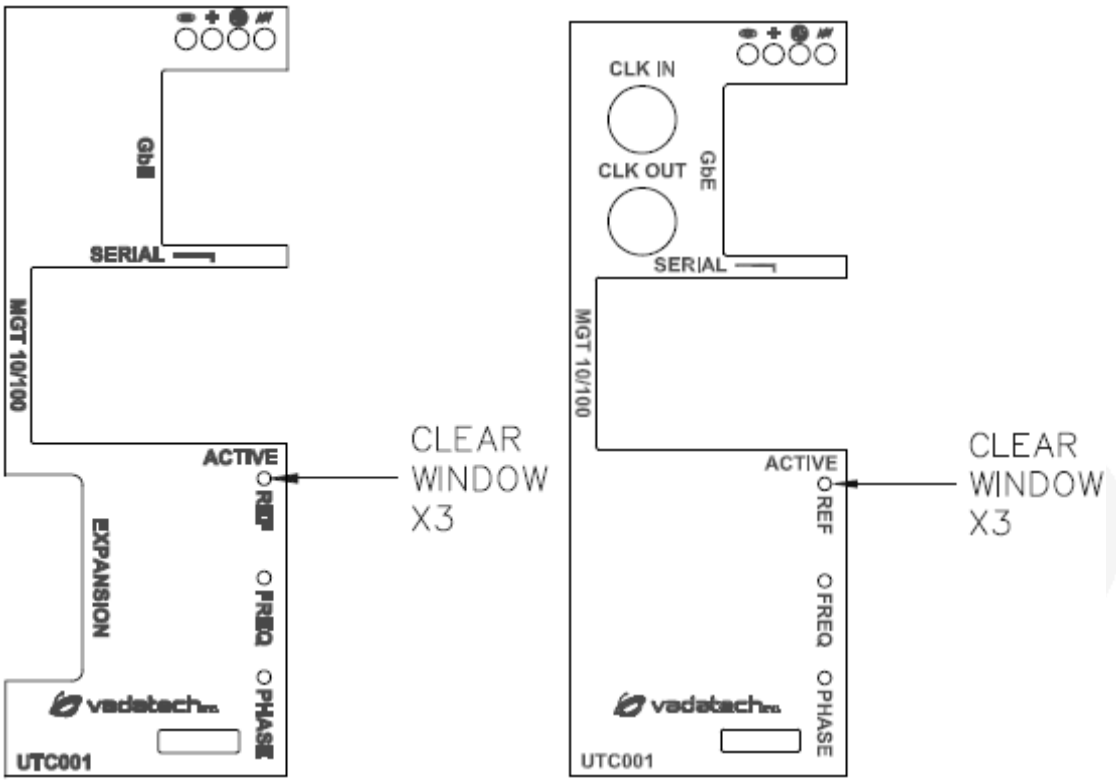

Figure 22: UTC001 front panel variations

The front panel on the left shows the Expansion port for the fabric DA (but not the SAS/SATA Expansion port) and without the CLK IN/CLK OUT ports.

The front panel on the right shows the CLK IN/CLK OUT ports but without the Expansion ports.

4.21 UTC002 Front Panel

The conceptual front panel of the UTC002 shown below consists of the MCH hot-swap handle, IPMI LEDs, RJ45 for IPMI Serial Console port, RJ45 for IPMI 10/100 Ethernet port, two RJ-45s for the GbE Switch, two SFP+ or two QSFP for expansion, SMB clock in/out for Telcom clocking, and various status LEDs. The figures below show the front panel connections with callouts to help clarify the purpose of connectors/LEDs:

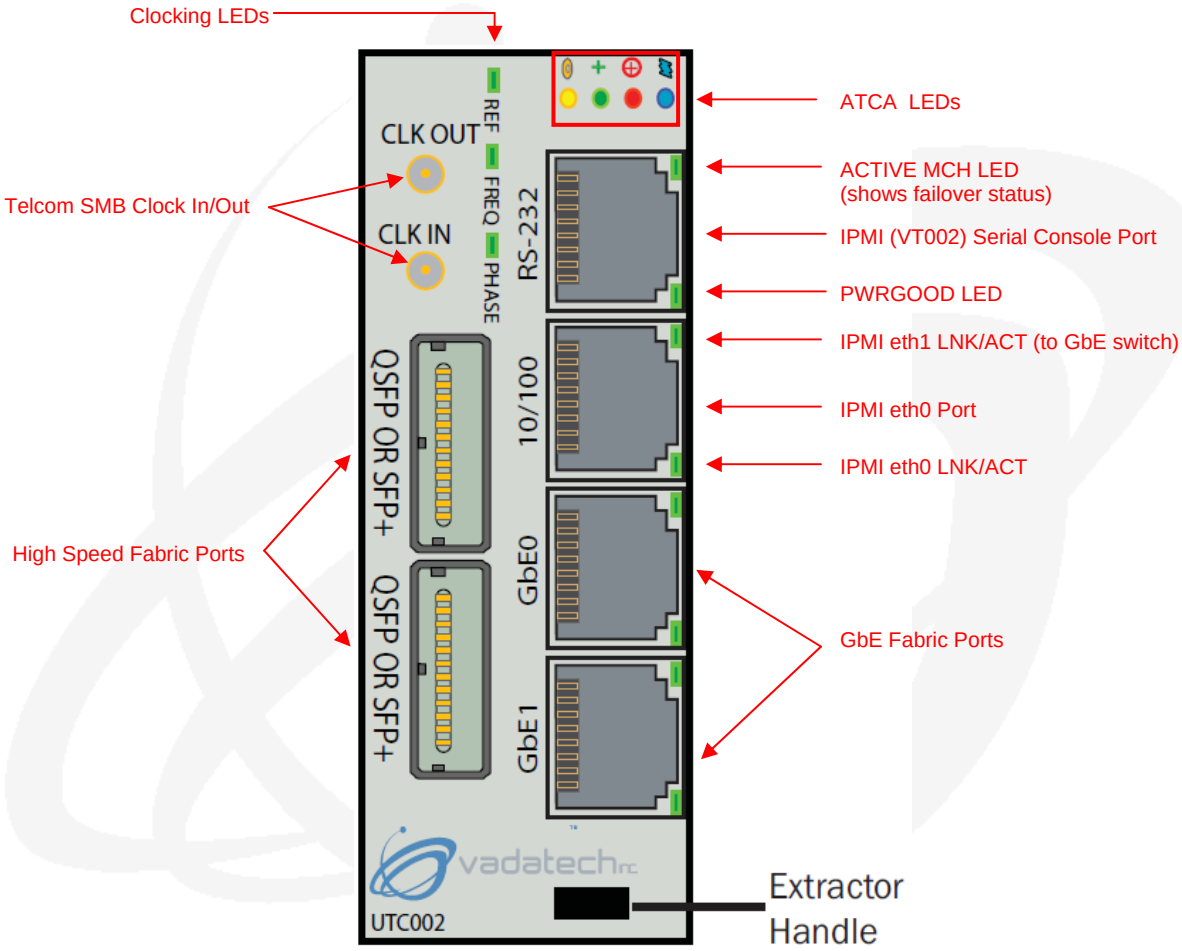

Figure 23: UTC002 front panel

4.22 UTC002 Front Panel Variations

The front panel of the UTC002 will depend on the combination of ordering options.

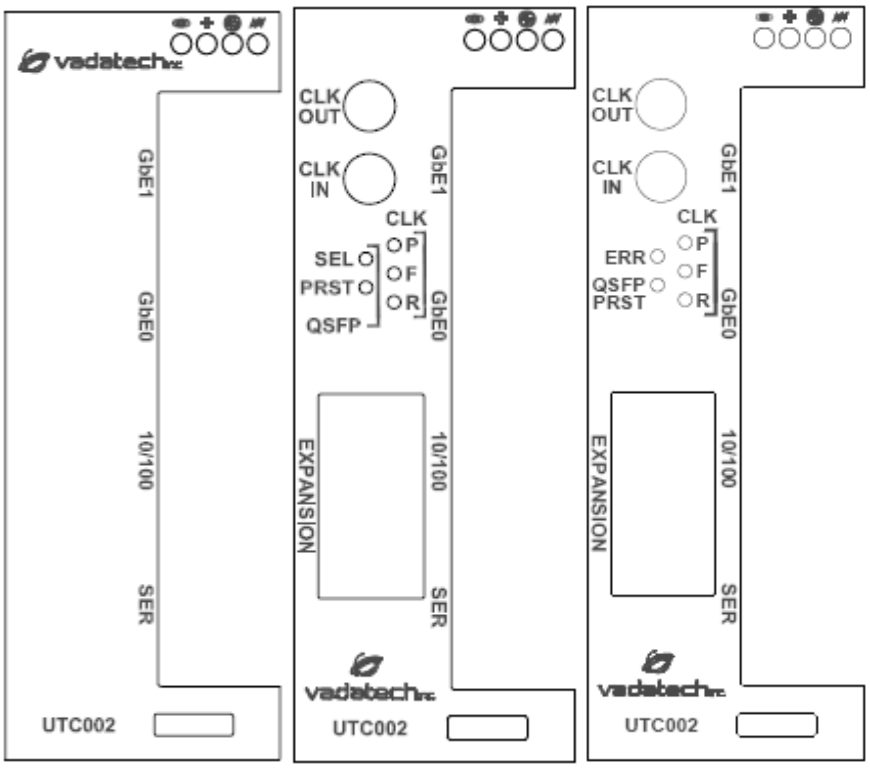

Figure 24: UTC002 front panel variations (set 1)

This first set of UTC002 front panel variations show the 'No Fabric/No Clocking' variation on the left. This is the simplest possible UTC002 variation.

The middle variation is for PCIe and SRIO Gen1 Fabrics with the original style CLK IN / CLK OUT clocking I/O. The Fabric LEDs grouped as 'QSFP' are:

SEL (green): This LED corresponds to the QSFP "Module Select". When lit it indicates that the fabric chip has selected the QSFP module for communication via I2C.

PRSNT (green): This LED corresponds to the QSFP "Module Present". When lit it indicates that the QSFP+ module has been detected as present by the board.

The right variation is for SRIO Gen2 with the original style CLK IN / CLK OUT clocking I/O. The Fabric LEDs are:

ERR (red): When lit this LED indicates that an error condition has been signaled from the SRIO fabric chip to the management processor.

QSFP PRST (green): This LED corresponds to the QSFP "Module Present". When lit it indicates that the QSFP+ module has been detected as present by the board.

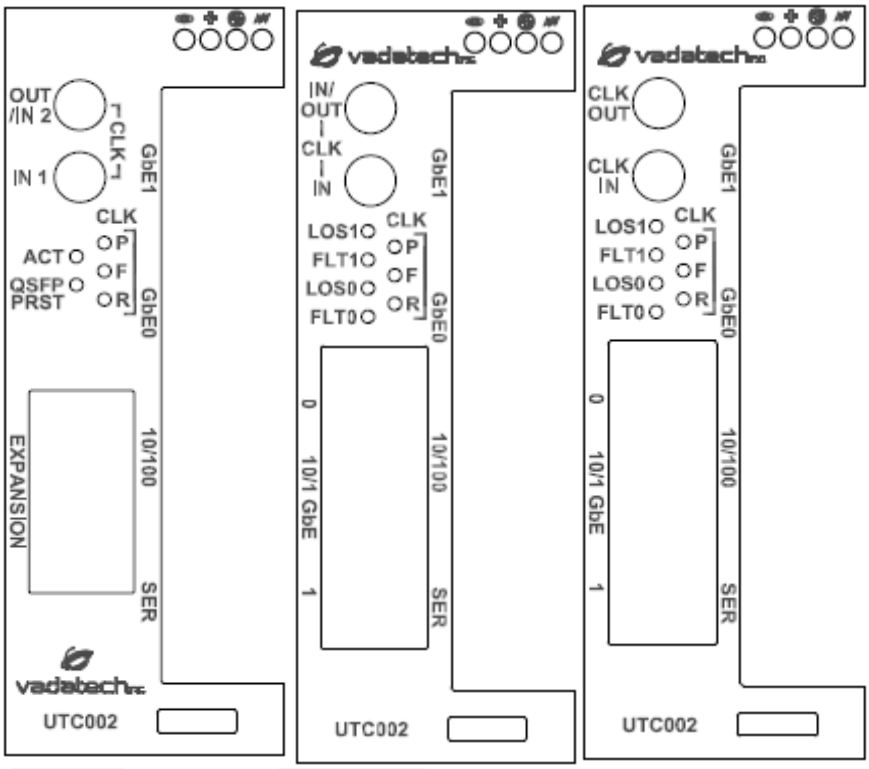

Figure 25: UTC002 front panel variations (set 2)

The front panel variation shown on the left is for the CBS Fabric and has the newer style CLK IN / CLK OUT/IN2 clocking I/O. The Fabric LEDs are:

ACT (green): When configured, this LED shows activity at the SENSE output of the CBS. (This is not usually configured.)

QSFP PRST (green): This LED corresponds to the QSFP "Module Present". When lit it indicates that the QSFP+ module has been detected as present by the board.

The last two show the 10GbE Fabric with two variations of clocking I/O. The middle one shows the newer CLK IN / CLK OUT/IN2 style while the right one shows the original CLK IN / CLK OUT style. The Fabric LEDs for both of these variations are:

LOS0/1 (green): These LEDs turn on when the corresponding SFP+ module is reporting optical "Receiver Signal Detect". If the LED turns off it indicates the absence of the incoming optical signal.

FLT0/1 (green): These LEDs turn on when the corresponding SFP+ module is NOT reporting a "Transmitter Fault". If the LED turns off it indicates a fault.

Refer to VadaTech MCH Clocking Configuration Guide for more discussion on clocking I/O.

4.23 The ATCA Management LEDs

Per the µTCA MCH specification there are four LEDs that are opposite the handle and are controlled by the IPMI management controller. These four ATCA LEDs are colored Blue, Green, Amber/Yellow and Red. The Blue indicates the hot-swap state of the MCH. Initially, the Blue LED is on. When the MCH handle is closed upon insertion, and acknowledge by the carrier, the blue LED will blink (long blink). When the MCH has been powered up by the carrier, the blue LED will go off indicating that the MCH is fully operational in the system. If the AMC handle is opened, starting a removal sequence, and acknowledged by the carrier the blue LED will blink (short blink) until the MCH has been completely powered down at which point the blue LED will be continuously lit. This indicates to the operator that it is safe to remove the MCH from the chassis.

Name	Color	Description
Hotswap	Blue	hotswap state, per PICMG AMC.0 and MicroTCA specifications
Error	Red	ON indicates failure has occurred on the UTC001/UTC002 OFF indicates normal operation
Health	Green	ON indicates normal operation OFF indicates a failure has occurred on the UTC001/UTC002
Application	Amber	is not currently being used

Table 20: UTC001/UTC002 ATCA LEDs

4.24 Insertion/Removal Mechanism

The UTC001/UTC002 is a hot-plugged FRU, which allows it to be inserted into the chassis while the system is up. The UTC001/UTC002 could also be removed live from the system. The front panel handle is pulled outward to notify the hot removal. The blue light starts blinking, which during this time the module must not be removed. The IPMI Management controller notifies the carrier of the intention of removing the module. The solid Blue light is an indicator that it is safe to remove the Module.

For more information on UTC001/UTC002 Hotswap States please refer to the VadaTech MicroTCA software manuals.

4.25 Port Pin-outs

The **MGT 10/100** port is pinned out in compliance with 100BASE-T.

The **GbE** ports are pinned out in compliance with 1000BASE-T.

The **SERIAL/RS-232** port is pinned out as follows:

Pin #	Pin Description
1	(no connect)
2	TX of IPMI Controller (RS-232)
3	RX of IPMI Controller (RS-232)
4	(no connect)
5	GND
6	(no connect)
7	(no connect)
8	(no connect)

Table 21: Serial port pin out

The SAS/SATA, PCIe, SRIO, 10GbE (XAUI), and CBS expansion ports on the UTC001 are pinned out as follows and carry the SERDES signals for the corresponding bus standard:

Pin #	Pin Description	Pin #	Pin Description
A1	GND	B1	GND
A2	RX0+	B2	TX0+
A3	RX0-	B3	TX0-
A4	GND	B4	GND
A5	RX1+	B5	TX1+
A6	RX1-	B6	TX1-
A7	GND	B7	GND
A8	RX2+	B8	TX2+
A9	RX2-	B9	TX2-
A10	GND	B10	GND
A11	RX3+	B11	TX3+
A12	RX3-	B12	TX3-
A13	GND	B13	GND

Table 22: UTC001 Expansion ports pin out

For description of the CLK IN / CLK OUT/IN2 ports, refer to the VadaTech MCH Telco / GPS Clock Configuration Guide.

The UTC002's SFP+ 10GbE expansion ports conform to the SFP+ MSA specification. More details on these ports can be found in the VadaTech 10GbE Switch Management Console Guide.

4.26 Switch settings

There are a number of switch settings within the UTC001 module, however all of the switches are pre-configured during manufacturing and their settings should not be changed by the customer.

4.27 Software

Please refer to the VadaTech MicroTCA MCH Getting Started Guide (& related software manuals) for complete description of the software behavior and user interfaces available for configuration and monitoring of the MCH.

4.28 Additional Specifications

Please refer to the UTC001/UTC002 Datasheet for detailed environmental, conformance, and warranty specifications.

5 Appendix A: UTC001/UTC002 Ethernet Connectivity

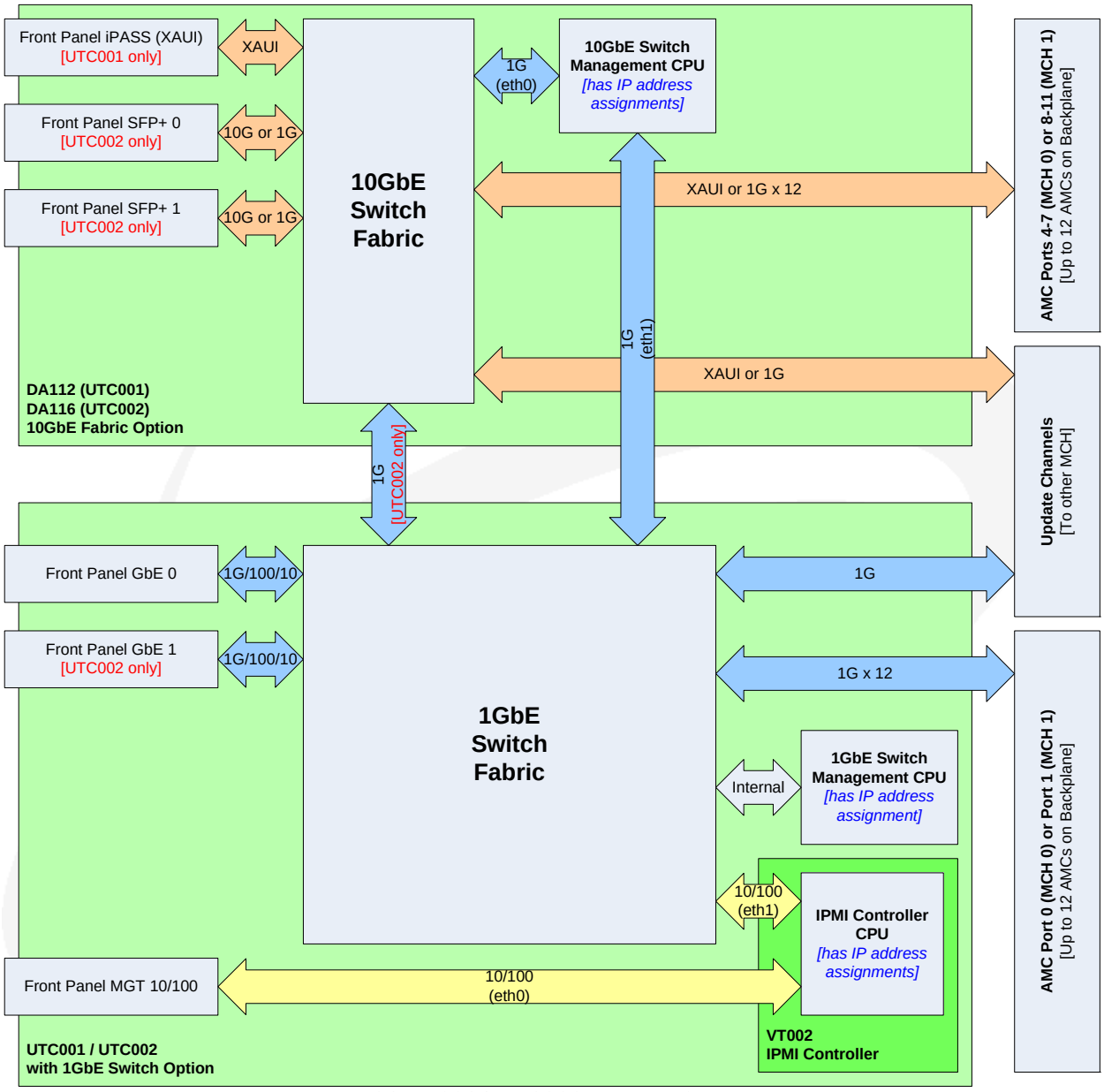

Figure 26: UTC001/UTC002 Ethernet Connectivity

NOTE: When configuring the MCH, all blocks shown as having IP address assignments must be independently configured to comply with your desired backplane and external IP address plan. Also, the switches may need further configuration for various features such as RSTP or the configuration of link speeds or to disable links, etc. Please refer to the document references at the beginning of this document to find further details on the configuration for each block.

6 Appendix B: UTC001/UTC002 Backplane Pin-out

The UTC001/UTC002 boards are pinned out in compliance with the PICMG uTCA specification and strive to provide options for flexible system configuration. The differences in the pin-outs corresponds changes to Tongue 2 signals only. Please refer to the PICMG uTCA specification and the UTC001/UTC002 base block diagram at the start of this manual while reading this section.

The UTC001/UTC002 support the 'default' uTCA pinning (Table 6-10 in the specification) when you select the Fabric B Ports Configuration option G=3 [No clocks – all Fabric B (SAS)]. This option allows all 12 AMCs to get SAS/SATA connectivity but does not distribute a CLK3/FCLKA to the AMCs.

The UTC001/UTC002 support two different '3 clock, partial Fabric' uTCA pin-outs (left side of Table 6-11 in the specification), the first one is option G=1 [Fabric clock shared with Fabric B (SAS)]. This option provides SAS/SATA connectivity to AMCs 1-6 but borrows the SAS/SATA channels for AMCs 7-12 so that a fabric clock (on CLK3/FCLKA) can be distributed to all 12 AMCs. This option is typically selected for PCIe fabric (D=1 or D=5) and usually implies that the Fabric Clock option (F=1) should also be selected.

The second '3 clock, partial Fabric' uTCA pin-out is option G=2 [Telcom clock shared with Fabric B (SAS)]. This option provides SAS/SATA connectivity to AMCs 1-6 but borrows the SAS/SATA channels for AMCs 7-12 so that a telcom clock (on CLK3/FCLKA) can be distributed to all 12 AMCs. This option is typically selected with one of the Telcom/GPS Clock options E=1, 2, 3, 4, or 5.

NOTE: The UTC001/UTC002's Fabric Clock and Telcom Clock functional blocks are completely independent of each other except for the possible pin-out conflicts shown above. The Fabric Clock option cannot route Telcom clocks and the Telcom option cannot route Fabric Clocks. Therefore it is important that the proper option be chosen up front.

IMPORTANT: *You must match your chassis/backplane ordering options with the MCH's ordering options so that the signaling on each side of the connector will match!*