VadaTech FMC228

Hardware Reference Manual

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vadatech inc

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Revision History

Doc Rev	Description of Change	Revision Date
1.1.0	Changed Pin-out (LMK04828 DCLKOUT4/6) for Rev. B board	5/20/2016
1.0.0	Split out manual from original FMCs User Manual document.	3/23/2016

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Tables

1 Overview

This document details the FMC228 card; explaining its features, front panel, pin-outs, voltage requirements, etc.

NOTE: In the descriptions for I/O signals in this manual the input vs. output notation is from the FMC's perspective, not from the FPGA's perspective. When creating the FPGA I/O structures you will need to use the reverse directionality from what is shown in this manual.

1.1 Applicable Products

- VadaTech FMC228 (Quad 1GSps ADC)

1.2 Document References

- ANSI/VITA 57 FPGA Mezzanine Card Standard
- VadaTech FMC228 Datasheet
- TI LMK04828B Datasheet (JESD204B PLL found on FMC225/FMC226/FMC228)
- Hittite HMC835LP6GE Datasheet (Freq Synth found on FMC226/FMC228)
- Analog Devices AD9234 Datasheet (ADC found on FMC228)

1.3 Acronyms Used in this Document

Acronym	Description
ADC	Analog-to-Digital Converter
AMC	Advanced Mezzanine Card
CPU	Central Processing Unit
EEPROM	Electrically Erasable Programmable Read Only Memory
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
HA	HPC 'A' bank (up to 24 differential pairs/48 single-ended)
HB	HPC 'B' bank (up to 22 differential pairs/44 single-ended)
HPC	High Pin Count
LA	LPC 'A' bank (up to 34 differential pairs/68 single-ended)
LPC	Low Pin Count
LVDS	Low-Voltage Differential Signaling
MMC	Module Management Controller
PLL	Phase Locked Loop
SERDES	Serializer/Deserializer
VADJ	'A' bank Adjustable Voltage (provided by carrier to mezzanine)
VIO_B_M2C	'B' bank I/O Voltage (provided by mezzanine to carrier)
VREF_A_M2C	'A' bank reference voltage (provided by mezzanine to carrier)
VREF_B_M2C	'B' bank reference voltage (provided by mezzanine to carrier)

Table 1: Acronyms

2 Common FMC Features / Cautions

The VadaTech FMCs follow the ANSI/VITA FPGA Mezzanine Card specification (ANSI/VITA57). Please familiarize yourself with the specification document before undertaking an FPGA design targeting one of the VadaTech FMCs.

All VadaTech FMCs feature the High Pin Count (HPC) FMC connector which is also compatible with the Low Pin Count (LPC) FMC connector. In accordance with the standard they all indicate their presence to the carrier board and expect it to provide the VADJ voltage specified in the on-board EEPROM. The EEPROM is to be read out while the +3.3VAUX is provided prior to VADJ being applied to the board.

The VadaTech FMC Carrier boards all have Module Management Controllers (MMCs) which take care of the task of reading the FMC's EEPROM, setting up the appropriate VADJ voltage, and sequencing power to both the payload (FPGA/CPU) and FMC. This allows the customer to focus on the payload design rather than on the management aspects of the carrier/module. Refer to the carrier's user manual for details on how to access the management interface which allows for viewing the EEPROM contents and setting up the power behavior of the board.

Due to the nature of the FMC mechanical design it is required that the AMC carrier's face plate be removed when installing or removing the FMC. Please refer to the AMC carrier's manual for more information on how to accomplish this and take care when assembling/disassembling the board combination. Removal of the VPX carrier's faceplate is not required as there is a board cutaway area allowing for insertion/removal.

NOTE: VadaTech's warranty does not cover damage caused by the customer during module mating/removal.

WARNING: The FMC specification enables mating of many different FMCs to many different carriers using the same connector in the interest of hardware design flexibility. However, each FMC + Carrier + FPGA logic design is a unique matched combination. The FMC must match the capabilities of the carrier in terms of voltage compatibility, and each FMC has a fixed pin-out which must match the FPGA logic design's pin-out (UCF file/HDL design). If all three of these do not match then physical damage could result (such as if an FMC output is also being driven as a carrier output by the FPGA). VadaTech's available FPGA reference designs target specific FMCs and are not compatible with other FMCs. When targeting a different combination of FMC + Carrier + FPGA logic design, make sure to remove the VadaTech FPGA configuration image from the board or set the image's pin mux to 'NO FMC' prior to mounting the new FMC. Damage caused by having mismatched FPGA/FMC I/O is not covered by the VadaTech warranty.

3 FMC228 Hardware

3.1 Overview

The FMC228 is Quad ADC board that includes the following key components:

- TI LMK04828B Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs
  - Feeds the ADC clock synthesizer with 100MHz
  - Provides SYSREFs and DCLKOUTs
- Hittite HMC835LP6GE Fractional-N PLL with Integrated VCO (33 – 4100MHz)
  - Feeds the ADC with max 4.1GHz
- Dual Analog Devices AD9234 12-bit 1GSps ADC with Integrated DDC
  - JESD204B 4-lane SERDES interface to the carrier FPGA per ADC chip

Please refer to the chip manufacturer's datasheets for additional technical details on these chips.

The on-board ADC sample clock generators take a reference clock from either the front panel or from the carrier board. The board also supports TRIG IN and TRIG OUT signaling.

Attribute	Value
Module Size	Single Width
Connector	HPC
VADJ	+1.2V through 3.3V
VIO_B_M2C	+1.2V through 3.3V *(tied to VADJ on FMC)*
VREF_A_M2C	(unused)
VREF_B_M2C	(unused)
Highest DP Lane #	7
Highest LA Pair #	25
Highest HA Pair #	n/a
Highest HB Pair #	n/a

Table 2: FMC228 Interface Specification

NOTE: The FMC228 incorporates level shifters for VADJ single-ended signals which can span the range shown in the previous table. However, it also uses LVDS differential signaling without level shifters. Please refer to your FMC carrier documentation to determine the proper VADJ voltage to use to allow the FPGA to implement the LVDS I/O standard with internal termination.

3.2 Block Diagram

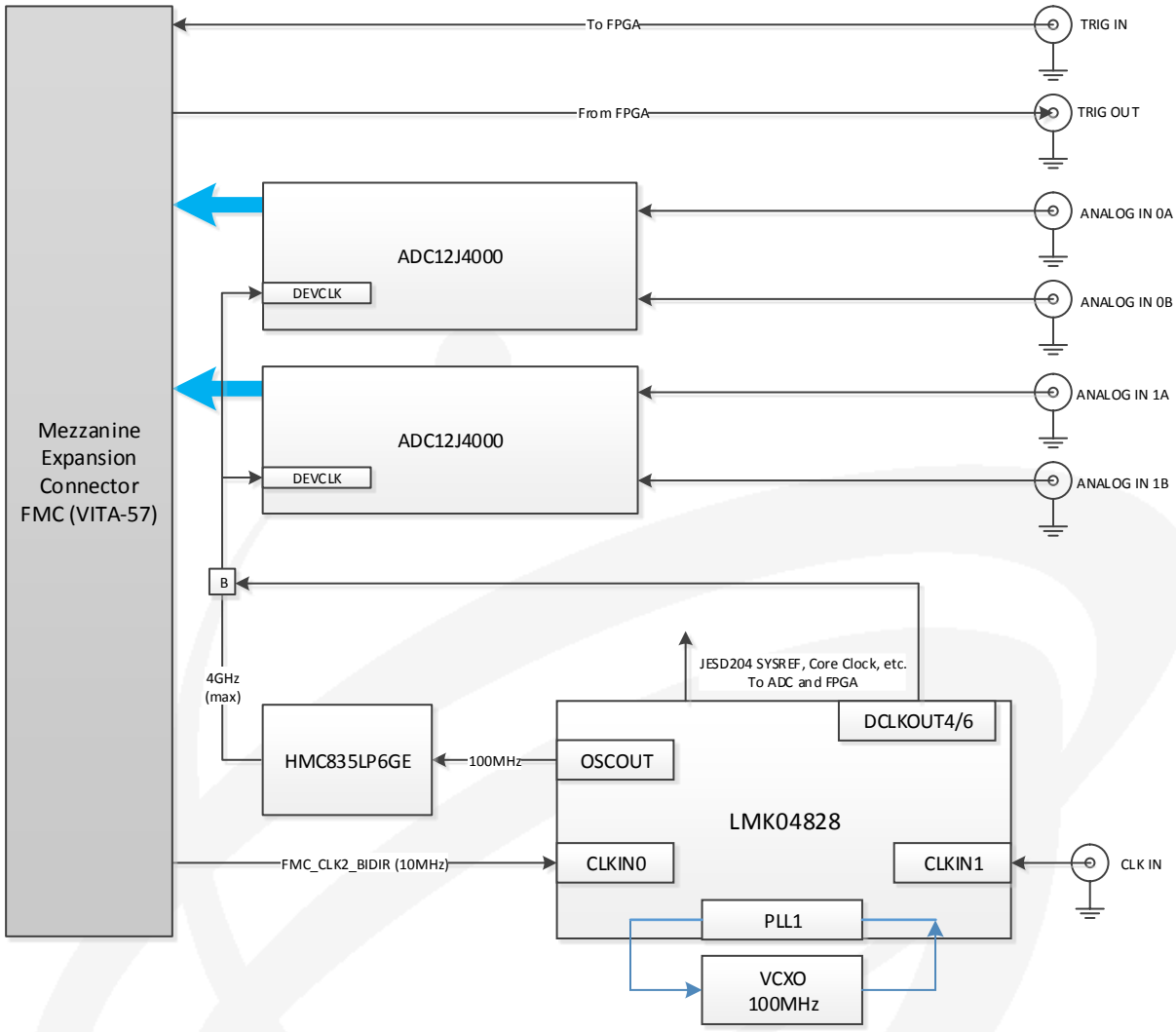

Figure 1: FMC228 Block Diagram

The block diagram shows boxes representing ordering option B. This option allows for the front panel CLK IN port to be either the reference clock for the PLL or used as the direct ADC clock. This option is installed at the time of manufacturing.

3.3 Front Panel

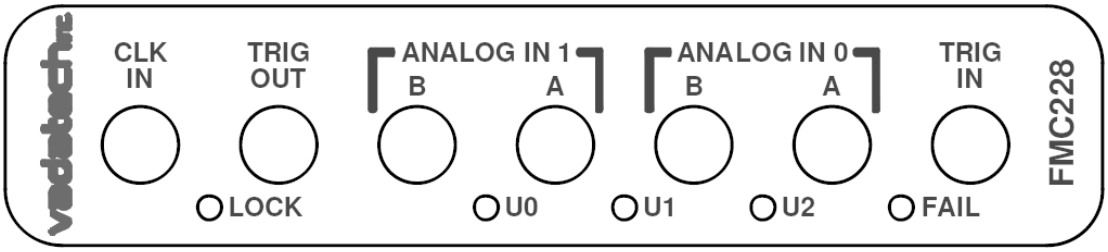

Figure 2: FMC228 Front Panel

The front panel of the FMC228 utilizes SSMC connectors for the following signals:

Connector	Direction	Voltage Range	Usage
CLK IN	Input	0V - +3.1V	Reference Clock or
TRIG OUT	Output	0V - +3.3V	Trigger Output from FPGA
ANALOG IN 1B	Input	Refer to ADC datasheet	ADC Input
ANALOG IN 1A	Input	Refer to ADC datasheet	ADC Input
ANALOG IN 0B	Input	Refer to ADC datasheet	ADC Input
ANALOG IN 0A	Input	Refer to ADC datasheet	ADC Input
TRIG IN	Input	0V - +3.3V	Trigger Input to FPGA

Table 3: FMC228 Connectors

A row of LEDs is provided on the front panel for status reporting:

Label	ON	OFF
LOCK	HMC PLL Locked	HMC PLL Unlocked
U0	User Defined	User Defined
U1	User Defined	User Defined
U2	User Defined	User Defined
FAIL	Local Power Fault	No Local Power Fault

Table 4: FMC228 Front Panel LEDs

Additional status LEDs are available on the PCB to help facilitate debugging of the LMK PLL:

Label	ON	OFF
DS5 (CLKIN SEL0)	User Defined	User Defined
DS6 (CLKIN SEL1)	User Defined	User Defined
DS7 (STATUS LD1)	User Defined	User Defined
DS8 (STATUS LD2)	User Defined	User Defined

Table 5: FMC228 On-board LEDs

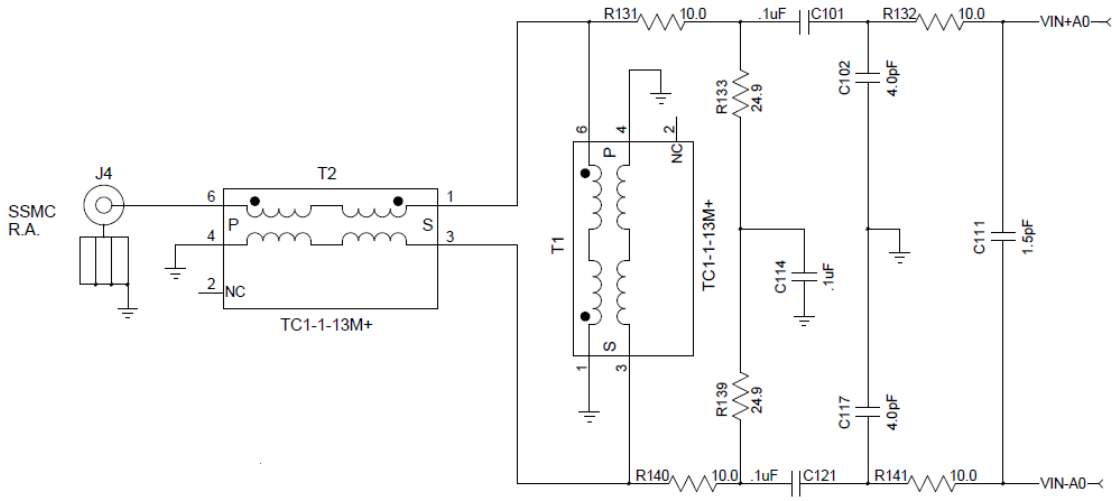

Figure 3: FMC228 ADC Input Circuit (typical)

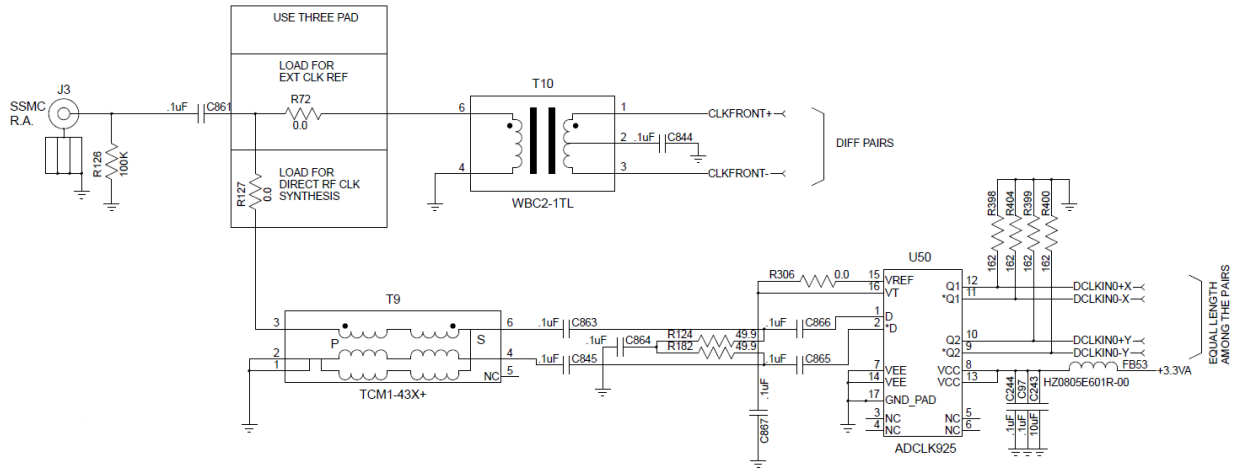

Figure 4: FMC228 Clock Input Circuit

3.4 PCB Layout

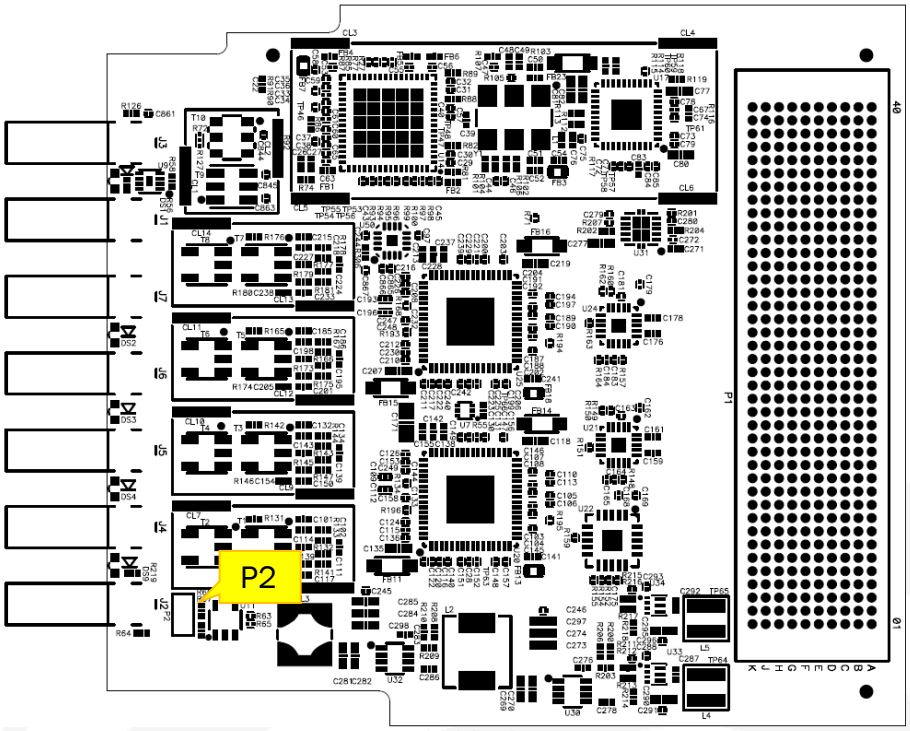

Figure 5: FMC228 PCB Layout

3.5 Configuration Jumpers

The FMC228 contains a header (P2) which allows for selection of a 50ohm termination of the TRIG IN port:

P2 Jumper Pins	Meaning
SHUNTED	TRIG IN with 50ohm termination
OPEN	TRIG IN without 50ohm termination

Table 6: FMC228 P2 Jumper Settings

3.6 Module Payload Inputs/Outputs

I/O	Dir	Type	Description
*ADCCS0	Input	Single-ended	ADC 0 Serial Chip Select (active low)
*ADCCS1	Input	Single-ended	ADC 1 Serial Chip Select (active low)
*LMKCLK_CS	Input	Single-ended	LMK04828 Serial Chip Select (active-low)
*SYNCIN0+/-	Input	LVDS	ADC 0 JESD204B LVDS Sync Input (active low)
*SYNCIN1+/-	Input	LVDS	ADC 1 JESD204B LVDS Sync Input (active low)
*U[2:0]	Input	Single-ended	User LED controls (active low)
10MHZ_FPGA+/-	Input	LVDS	Reference clock input from baseboard to LMK04828 CLKIN0
ADCSCLK0	Input	Single-ended	ADC 0 Serial Clock
ADCSCLK1	Input	Single-ended	ADC 1 Serial Clock
ADCSDIO0	In/Out	Single-ended	ADC 0 Serial Data
ADCSDIO0_DIR	Input	Single-ended	ADC 0 Serial Data Direction (LOW=To FPGA, HIGH=To ADC)
ADCSDIO1	In/Out	Single-ended	ADC 1 Serial Data
ADCSDIO1_DIR	Input	Single-ended	ADC 1 Serial Data Direction (LOW=To FPGA, HIGH=To ADC)
CLKOE	Input	Single-ended	Enable LMK04828's VCXO to output to the PLL OSCIN port
DCLKOUT0+/-	Output	LVDS	LMK04828 Device Clock for SERDES ref clock (GBTCLK0)
DCLKOUT10+/-	Output	LVDS	LMK04828 Device Clock for FPGA
DCLKOUT12+/-	Output	LVDS	LMK04828 Device Clock for FPGA
DCLKOUT2+/-	Output	LVDS	LMK04828 Device Clock for SERDES ref clock (GBTCLK1)
DP_M2C[3:0]+/-	Output	SERDES	ADC 0 SERDES output lanes
DP_M2C[7:4]+/-	Output	SERDES	ADC 1 SERDES output lanes
FD_A0	Output	Single-ended	ADC 0 Fast Detect Output for Channel A
FD_A1	Output	Single-ended	ADC 1 Fast Detect Output for Channel A
FD_B0	Output	Single-ended	ADC 0 Fast Detect Output for Channel B
FD_B1	Output	Single-ended	ADC 1 Fast Detect Output for Channel B
HMC_CHIP_EN	Input	Single-ended	HMC835LP6GE Chip Enable
HMC_LD0	Output	Single-ended	HMC835LP6GE Lock Detect GPIO (AUX0_SDO)
HMC_SCK	Input	Single-ended	HMC835LP6GE Serial Clock
HMC_SDI	Input	Single-ended	HMC835LP6GE Serial Data In
HMC_SDO	Output	Single-ended	HMC835LP6GE Serial Data Out (LD_SDIO)
HMC_SEN	Input	Single-ended	HMC835LP6GE Serial Enable
LMKCLKRESET	Input	Single-ended	LMK04828 Reset
LMKDIR/SDIO	Input	Single-ended	LMK04828 LMKSDIO direction control: LOW=To FPGA, HIGH=To PLL
LMKDIR/SYNC	Input	Single-ended	LMK04828 SYNC_SYSREF_REQ direction control: LOW=To FPGA, HIGH=To PLL
LMKSCLK	Input	Single-ended	LMK04828 Serial Clock
LMKSDIO	In/Out	Single-ended	LMK04828 Serial Data Input/Output
LMKSYNC/SYSREF_REQ	In/Out	Single-ended	LMK04828 Serial Sync/SYSREF_REQ/Programmable Status
PDWN/STBY0	Input	Single-ended	ADC 0 Power Down/Standby (active high)
PDWN/STBY1	Input	Single-ended	ADC 1 Power Down/Standby (active high)
STATUS_LD[2:1]	Output	Single-ended	LMK04828 Status
SYSREF11+/-	Output	LVDS	LMK04828 SYSREF to FPGA
SYSREF13+/-	Output	LVDS	LMK04828 SYSREF to FPGA
TRIG_IN+/-	Output	LVDS	Front panel TRIG IN via LVTTL-to-LVDS buffer
TRIG_OUT+/-	Input	LVDS	Front panel TRIG OUT via LVDS-to-LVTTL buffer

Table 7: FMC228 FMC Connector Inputs/Outputs (from FMC perspective)

3.7 FMC228 Pin-out

Pin	Column A	Column B	Column C	Column D	Column E
1	GND	+3.3V (PU)	GND	(open)	GND
2	DP1_M2C+	GND	(open)	GND	(open)
3	DP1_M2C-	GND	(open)	GND	(open)
4	GND	(GND)	GND	GBTCLK0_M2C_P (DCLKOUT0+)	GND
5	GND	(GND)	GND	GBTCLK0_M2C_N (DCLKOUT0-)	GND
6	DP2_M2C+	GND	DP0_M2C+	GND	(open)
7	DP2_M2C-	GND	DP0_M2C-	GND	(open)
8	GND	(GND)	GND	LA01_P_CC (SYSREF+13)	GND
9	GND	(GND)	GND	LA01_N_CC (SYSREF-13)	(open)
10	DP3_M2C+	GND	LA06_P (ADCSDIO0_DIR)	GND	(open)
11	DP3_M2C-	GND	LA06_N (ADCSDIO0)	LA05_P (*ADCCS0)	GND
12	GND	DP7_M2C+	GND	LA05_N (ADCSCLK0)	(open)
13	GND	DP7_M2C-	GND	GND	(open)
14	DP4_M2C+	GND	LA10_P (ADCSDIO1_DIR)	LA09_P (*ADCCS1)	GND
15	DP4_M2C-	GND	LA10_N (ADCSDIO1)	LA09_N (ADCSCLK1)	(open)
16	GND	DP6_M2C+	GND	GND	(open)
17	GND	DP6_M2C-	GND	LA13_P (*LMKCLK_CS)	GND
18	DP5_M2C+	GND	LA14_P (LMKSYNC/SYSREF_REQ)	LA13_N (LMKSCK)	(open)
19	DP5_M2C-	GND	LA14_N (LMKDIR_SDIO)	GND	(open)
20	GND	GBTCLK1_M2C_P (DCLKOUT2+)	GND	LA17_P_CC (DCLKOUT10+)	GND
21	GND	GBTCLK1_M2C_N (DCLKOUT2-)	GND	LA17_N_CC (DCLKOUT10-)	(open)
22	(open)	GND	LA18_P (SYSREF11+)	GND	(open)
23	(open)	GND	LA18_N (SYSREF11-)	LA23_P (TRIG_OUT+)	GND
24	GND	(open)	GND	LA23_N (TRIG_OUT-)	(open)
25	GND	(open)	GND	GND	(open)
26	(open)	GND	(open)	(open)	GND
27	(open)	GND	(open)	(open)	(open)
28	GND	(open)	GND	GND	(open)
29	GND	(open)	GND	(open)	GND
30	(open)	GND	SCL	TDI -> TDO	(open)
31	(open)	GND	SDA	TDO	(open)
32	GND	(open)	GND	+3P3VAUX	GND
33	GND	(open)	GND	(open)	(open)
34	(open)	GND	GA0	(open)	(open)
35	(open)	GND	+12V	GA1	GND
36	GND	(open)	GND	+3.3V	(open)
37	GND	(open)	+12V	GND	(open)
38	(open)	GND	GND	+3.3V	GND
39	(open)	GND	+3.3V	GND	VADJ
40	GND	(open)	GND	+3.3V	GND

Table 8: FMC228 Pin-out (Columns A-E)

Pin	Column F	Column G	Column H	Column J	Column K
1	PG_M2C	GND	VREF_A_M2C	GND	VREF_B_M2C
2	GND	(open)	*PRSNT_M2C	(open)	GND
3	GND	(open)	GND	(open)	GND
4	(open)	GND	(open)	GND	CLK2_BIDIR_P (10MHZ_FPGA+)
5	(open)	GND	(open)	GND	CLK2_BIDIR_N (10MHZ_FPGA-)
6	GND	LA00_P_CC (DCLKOUT12+)	GND	(open)	GND
7	(open)	LA00_N_CC (DCLKOUT12-)	LA02_P (TRIG_IN+)	(open)	(open)
8	(open)	GND	LA02_N (TRIG_IN-)	GND	(open)
9	GND	LA03_P (*SYNCIN0+)	GND	(open)	GND
10	(open)	LA03_N (*SYNCIN0-)	LA04_P (*SYNCIN1+)	(open)	(open)
11	(open)	GND	LA04_N (*SYNCIN1-)	GND	(open)
12	GND	LA08_P (FD_B0)	GND	(open)	GND
13	(open)	(open)	LA07_P (PDWN/STBY0)	(open)	(open)
14	(open)	GND	LA07_N (FD_A0)	GND	(open)
15	GND	LA12_P (FD_B1)	GND	(open)	GND
16	(open)	LA12_N (LMKCLKRESET)	LA11_P (PDWN/STBY1)	(open)	(open)
17	(open)	GND	LA11_N (FD_A1)	GND	(open)
18	GND	LA16_P (STATUS_LD1)	GND	(open)	GND
19	(open)	LA16_N (STATUS_LD2)	LA15_P (LMKDIR/SYNC)	(open)	(open)
20	(open)	GND	LA15_N (LMKSDIO)	GND	(open)
21	GND	LA20_P (HMC_SDO)	GND	(open)	GND
22	(open)	LA20_N (HMC_SDI)	LA19_P (HMC_CHIP_EN)	(open)	(open)
23	(open)	GND	LA19_N (HMC_SCK)	GND	(open)
24	GND	(open)	GND	(open)	GND
25	(open)	(open)	LA21_P (HMC_LD0)	(open)	(open)
26	(open)	GND	LA21_N (HMC_SEN)	GND	(open)
27	GND	LA25_P (*U2)	GND	(open)	GND
28	(open)	LA25_N (CLKOE)	LA24_P (*U0)	(open)	(open)
29	(open)	GND	LA24_N (*U1)	GND	(open)
30	GND	(open)	GND	(open)	GND
31	(open)	(open)	(open)	(open)	(open)
32	(open)	GND	(open)	GND	(open)
33	GND	(open)	GND	(open)	GND
34	(open)	(open)	(open)	(open)	(open)
35	(open)	GND	(open)	GND	(open)
36	GND	(open)	GND	(open)	GND
37	(open)	(open)	(open)	(open)	(open)
38	(open)	GND	(open)	GND	(open)
39	GND	VADJ	GND	VIO_B_M2C	GND
40	VADJ	GND	VADJ	GND	VIO_B_M2C

Table 9: FMC228 Pin-out (Columns F-K)