VadaTech AMC721

CPLD Manual

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Version 1.1

vadatech inc.
THE POWER OF VISION

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Revision History

Doc Rev	Description of Change	Revision Date
1.0	Document Created	1/23/2013
1.1	Changed from SW4-4 to SW4-3 for consistency among products.	2/26/2013

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Figures

Tables

1 Overview

This document describes the functional behaviors of the AMC721 CPLD especially with respect to the various LED display modes supported.

1.1 Applicable Products

- AMC721

1.2 Document References

- AMI BIOS Documentation (for Port 0x80 POST codes)
- Intel Gladden/Cave Creek Documentation (for Power Sequencing)

1.3 Acronyms Used in this Document

Acronym	Description
AMC	Advanced Mezzanine Card
BIOS	Basic Input Output System
CPLD	Complex Programmable Logic Device
DIP	Dual In-line Package
ETH	Ethernet
GbE	Gigabit Ethernet
LED	Light Emitting Diode
PCH	Platform Controller Hub
PGOOD	Power Good
PHY	Physical Layer Device
POST	Power-On Self-Test
SATA	Serial ATA

Table 1: Acronyms

2 CPLD Functions

The AMC721 CPLD performs the following functions:

- Board-level reset sequencing
- Board-level power sequencing
- BIOS POST code (Port 0x80) two-digit seven-segment decode/display
- Front panel LED display
- SPI Flash programming mode via header w/ special LED display mode
- Power state debug special LED display mode

The board-level reset and power sequencing is implemented in compliance with the Intel requirements for the Gladden/Cave Creek chipset.

The BIOS POST code decode/display is compliant with typical port 0x80 display cards or on-mainboard displays that are found on Intel PCs.

SPI Flash programming mode is activated whenever a jig programming cable is connected to header J12. The cable is detected by the CPLD when pin 8 of the connector is grounded by the cable. When this occurs the CPLD disconnects the SPI Flash chips (containing the BIOS images) from the chipset so that an external SPI master can take control and program the chips. This mode requires a special sequence to activate properly:

1) Turn on the board without the SPI jig cable connected. The CPLD will start up and go through the power sequence to power up the SPI chips.
2) Attach the SPI jig cable. The CPLD will disconnect the SPI chips from the chipset and allow the external SPI master control over the SPI Flash chips.

NOTE: If the SPI jig cable is plugged in prior to power-up then the CPLD will not start up and the board will not power.

The LED display modes are described in the following sections.

3 Front Panel LED Display Modes

The front panel of the AMC721 is shown below:

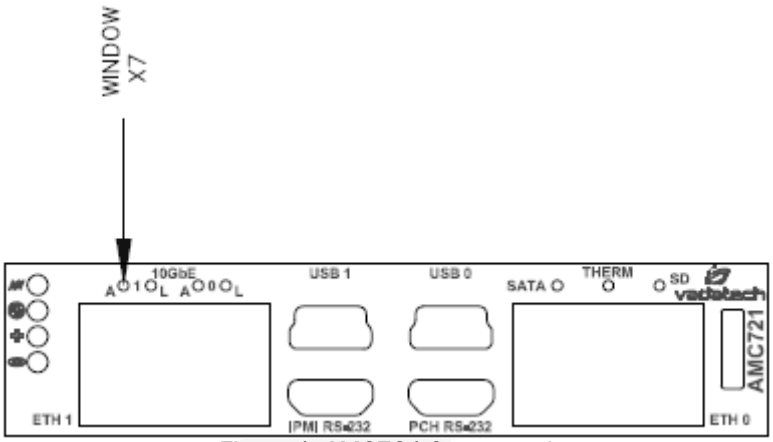

Figure 1: AMC721 front panel

The LEDs on the front panel controlled by the CPLD are:

ETH0: Yellow and Green LEDs as part of the RJ45 connector
ETH1: Yellow and Green LEDs as part of the RJ45 connector
SATA: Green LED

These LEDs behave differently based on the setting of SW4-3:

LED	SW4-3 OFF (Normal)	SW4-3 ON (Power State Debug)
ETH 1 Yellow	ETH 1 Status from PHY	SLP S5 asserted by PCH to CPLD
ETH 1 Green	ETH 1 Status from PHY	WDT TOUT asserted by PCH to CPLD
ETH 0 Yellow	ETH 0 Status from PHY	SLP S3 asserted by PCH to CPLD
ETH 0 Green	ETH 0 Status from PHY	SLP S4 asserted by PCH to CPLD
SATA	SATA activity from PCH	RSMRST asserted by CPLD to PCH

Table 2: Front panel LEDs controlled by CPLD

4 Seven Segment Display Modes

The bottom of the AMC721 includes two seven segment displays as shown below:

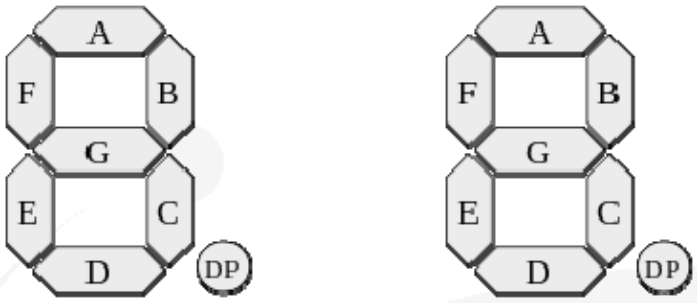

Figure 2: DS13 and DS14 seven segment displays

The seven segment displays have three distinct modes of operation:

1) Power State Debug display (SW4-3 ON)
2) BIOS POST code display (SW4-3 OFF - Default)
3) SPI Flash Programming display (SPI jig cable connected at J12)

4.1 Power State Debug Display

The Power State Debug display does not display hexadecimal numbers on the LEDs but instead uses each segment of the display as a unique LED to show a particular status line as being asserted (ON) or de-asserted (OFF).

LED	Status	LED	Status
DS13-A	PGOOD 3.3V	DS14-A	PGOOD VTT (SA CPU)
DS13-B	PGOOD 1.8V	DS14-B	PGOOD 1.2V
DS13-C	PGOOD 1.0V	DS14-C	PGOOD 2.5V
DS13-D	PGOOD 1.05V	DS14-D	PGOOD VCCP
DS13-E	PGOOD 1.5V (PCH)	DS14-E	PCH SYS PWROK asserted by CPLD to PCH
DS13-F	PGOOD 1.5V (Main)	DS14-F	PCH_PLTRSTX reset released by PCH
DS13-G	PGOOD VTT (Main)	DS14-G	PGOOD asserted by CPLD to board

Table 3: Power State Debug LEDs on seven segment display

In this mode the left decimal point lights if the PCH is in suspend mode (i.e. not fully powered up yet) and the right decimal point lights if the payload reset is asserted.

NOTE: A ‘fully up’ power state is displayed as ‘88’ with neither decimal point lit and none of the CPLD-controlled LEDs on the front panel lit (see previous section).

4.2 BIOS POST Code Display

In the BIOS POST code display mode a two-digit hexadecimal number is displayed. This number defaults to '00' at CPLD start-up and can be changed by the BIOS with writes to port 0x80.

In this mode the left decimal point lights if the PCH is in suspend mode (i.e. not fully powered up yet) and the right decimal point lights if the payload reset is asserted.

Refer to the AMI BIOS manuals for meanings of the BIOS POST codes.

4.3 SPI Flash Programming Display

In the SPI Flash Programming display mode a two-digit hexadecimal number is displayed whenever activity is detected on the SPI bus from the external SPI master. The number will display '00' if activity is seen destined for the SPI Flash attached to chip select 0 and the number will display '01' if activity is seen destined for the SPI Flash attached to chip select 1. If no activity is seen for 128ms then the display will blank.

In this mode the left decimal point blinks rapidly at a rate of ~8 Hz as an indication that the board is in SPI Flash Programming mode and the SPI Flash chips are connected to the external SPI master via the jig connector and not the PCH (meaning that the CPU can't boot the BIOS in this mode). The right decimal point lights if the payload reset is asserted.