VadaTech AMC72X

User's Manual

November 20, 2015

Version 2.9.8

vadatech inc

THE POWER OF VISION

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Revision History

Doc Rev	Description of Change	Revision Date
1.0.0	Document Created	3/26/2013
1.2.0	Updated Serial over lan	4/20/2013
1.3.0	Added network device mapping section	5/20/2013
1.4.0	Updated Default Switch Settings	6/14/2013
1.5.0	Updated Network boot (PXE) configuration instructions	6/19/2013
1.6.0	Added instructions for AMI AFU BIOS upgrade	6/26/2013
1.7.0	Updated Linux software section	8/22/2013
1.8.0	Changed SW3-4 default to Off (On-Board Clock)	2/01/2014
1.9.0	Added Graceful shutdown section	4/11/2014
2.0.0	Updated with AMC725 related information	04/30/2014
2.1.0	Added VNC server support	08/09/2014
2.2.0	Updated BIOS upgrade section	12/16/2014
2.3.0	Updated Graceful shutdown section Added AMC deactivation section	01/23/2015
2.4.0	Added "Recommended Sanitizing Procedures" section	02/05/2015
2.5.0	Added "Watchdog configuration" section	02/18/2015
2.6.0	Update BIOS section to reference the file names in the package	02/25/2015
2.7.0	Updated BIOS upgrade command	03/04/2015
2.8.0	Updated "Graceful Shutdown Support " section	04/16/2015
2.9.0	Added "Auto-negotiation Capability" section	04/24/2015
2.9.1	Fixed argument for ethtool sample	04/24/2015
2.9.2	Added sensors table information	05/15/2015
2.9.3	Updated network interface naming Added SD Card restoring steps with Clonezilla image	05/19/2015
2.9.4	Added Network Device Mapping table for AMC725. Updated Front0/Front1 1GbE port names to ETH0/ETH1 for AMC720, AMC721, AMC722, AMC723	06/01/2015
2.9.5	Updated SD Card restoring steps with Clonezilla image to boot using serial console.	10/28/2015
2.9.6	Updated note on SW4-4	10/29/2015
2.9.7	Updated steps for making bootable USB for Clonezilla.	11/13/2015
2.9.8	Added bsp-version command info. Added note for payload BSP memory allocation size.	11/20/2015

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Tables

Overview

The AMC72X are Processor AMC (PrAMC) modules in a single or double-width (based on model), mid or full-height AdvancedMC (AMC) form factor based on the Intel® next generation Core i Processor (Gladden) with Cave Creek PCH

This document describes the VadaTech AMC72X boards and their use as a development platform.

This boards feature:

- Intel Gladden processor options for 1, 2 or 4 cores
- Core speed options ranging from 1 GHz to 2GHz
- Options for 4GB, 8GB, or 16GB of DDR3 ECC memory (dual slot/single controller)
- PCIe, SRIO or XAUI to the backplane fabric 4-7 and 8-11
- Four 1GbE ports
    - Two dedicated as 1000Base-X AMC Port 0 and Port 1
    - Two dedicated as ETH0 and ETH1 front 10/100/1000Base-T ports
- SD card slot on-board for file system storage (USB2244)
- 8MB of boot flash memory standard (AT25DF321A)
- Dual SATA Ports to AMC Port 2 and Port 3
- Dual USB on the front panel
- Real-time Clock with battery backup
- RS-232 serial console on the front panel
- On-board AMC MMC IPMI management controller
- Serial Over LAN (SOL) – Gladden console via the MMC IPMI Ethernet on one of four 1GbE Ports (software configurable from CLI)
- Hardware random number generator for enhanced SOL cryptographic security

Applicable Products

- VadaTech AMC720
- VadaTech AMC721
- VadaTech AMC722
- VadaTech AMC723
- VadaTech AMC725

Document References

- PICMG AMC.0 (base) standard

- PICMG AMC.1 (PCIe) standard
- PICMG AMC.2 (Ethernet) standard
- PICMG AMC.4 (SRIO) standard
- VadaTech AMC72X Datasheet

Acronyms Used in this Document

Acronym	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telephony Computing Architecture
BSP	Board Support Package
CPU	Central Processing Unit
DDR	Double Data Rate
DIP	Dual In-line Package
ECC	Error Correction Coding
GB	Gigabyte
GbE	Gigabit Ethernet
GHz	Gigahertz
GND	Ground
IPMI	Intelligent Platform Management Interface
LED	Light Emitting Diode
MAC	Media Access Controller
MHz	Megahertz
MMC	Module Management Controller
PCIe	Peripheral Component Interconnect Express
PrAMC	Processor AMC
SHLD	Shield
USB	Universal Serial Bus
*u*TCA	Micro Telephony Computing Architecture
XAUI	10 Gigabit Media Independent Interface

Table 1: Acronyms

Hardware Overview

Block Diagram

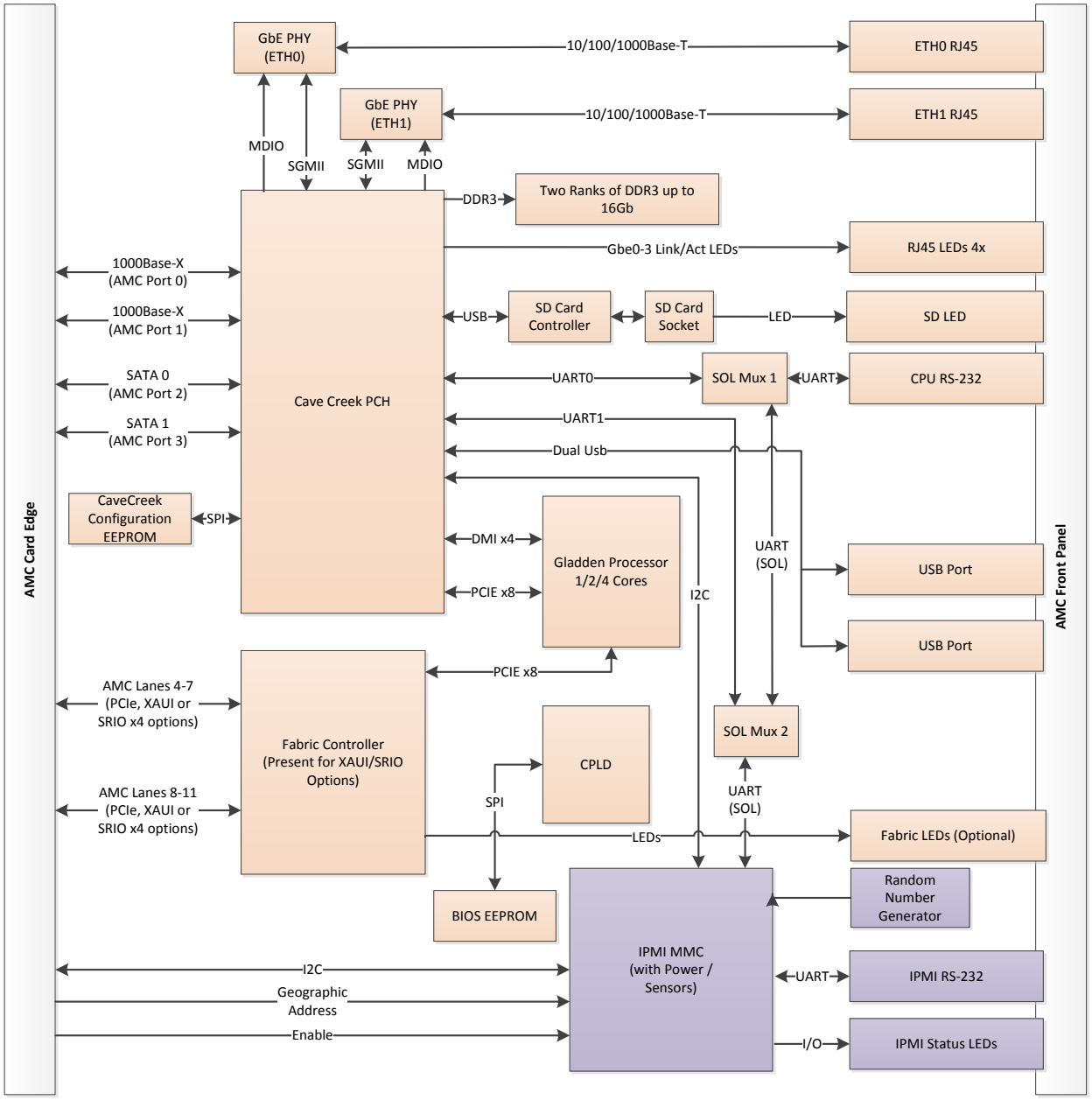

Figure 1: AMC72X (applicable to X=0, 1, 2, and 3) Block Diagram

Board Layout

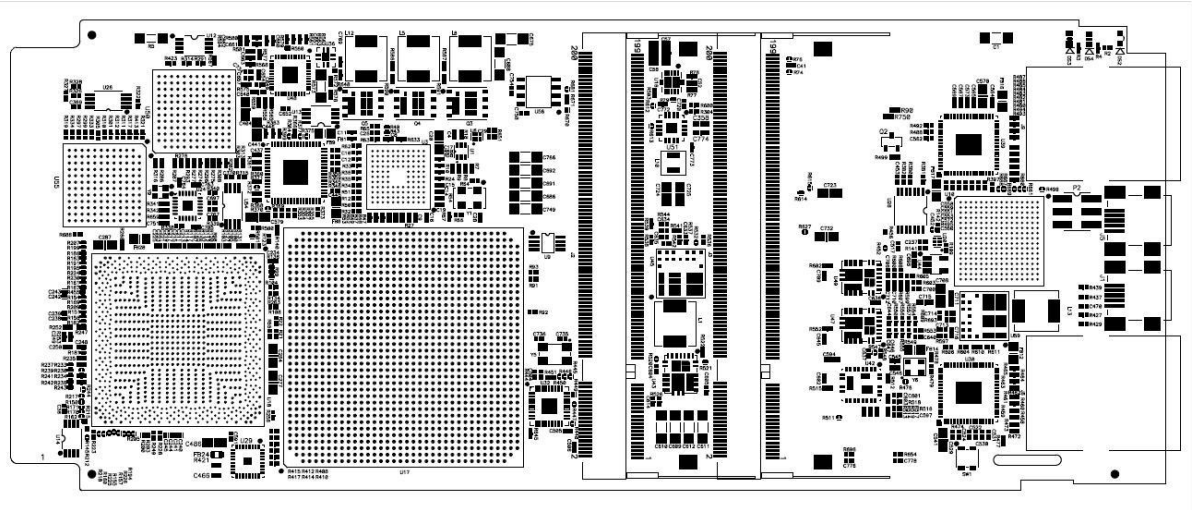

Figure 2: AMC72X Top Layout (front to the left) (X=0, 1, 2, and 3)

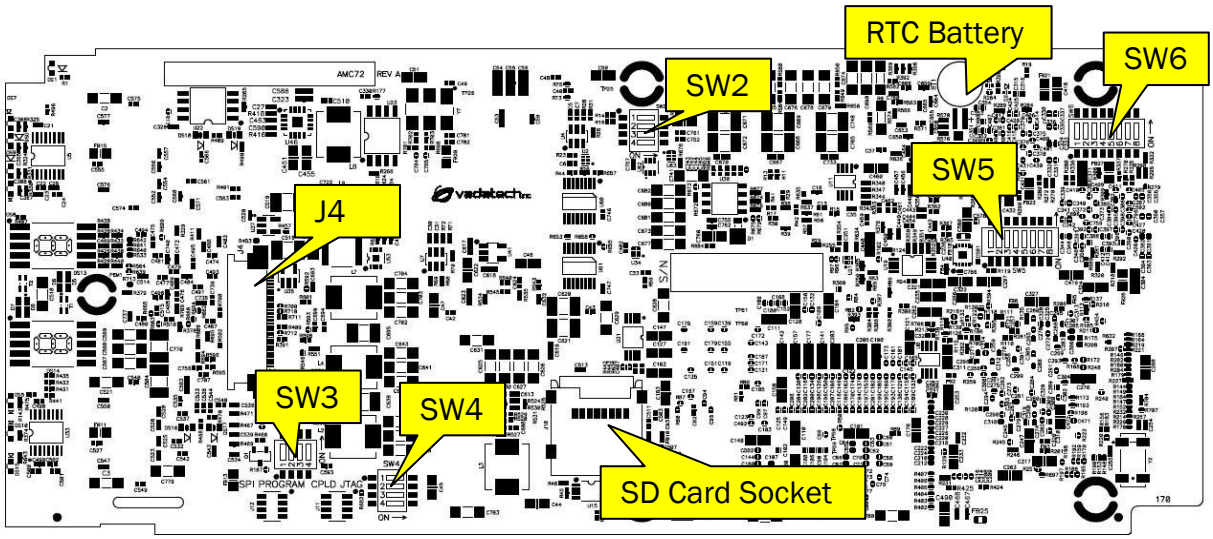

Figure 3: AMC72X Bottom Layout (front to the left) (X=0, 1, 2, and 3)

DIP Switches SW2, SW3, and SW4 are common to all AMC72X boards, switches 5 and 6 are applicable only for AMC722.

SWITCHES	DESCRIPTION
SW2	IPMI Related Functions
SW3	Misc Configuration Switches
SW4	Misc Configuration Switches
SW5	SRIO Ports 4-7 Options
SW6	SRIO Ports 8-11 Options

Table 2: AMC72X Switch configurations

Front Panel Layouts

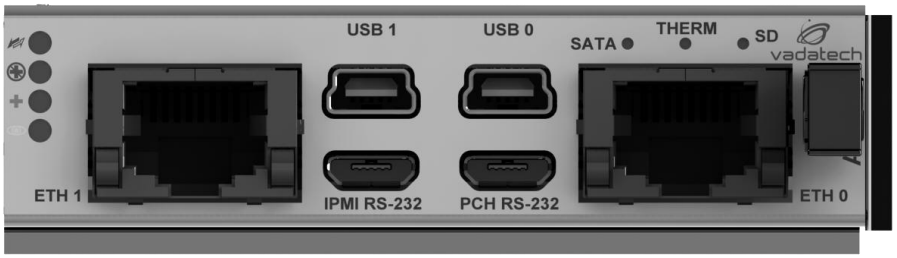

Figure 4: AMC720 Front Panel

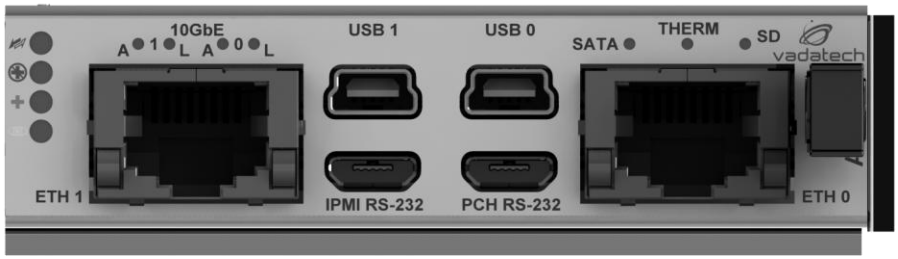

Figure 5: AMC721 Front Panel

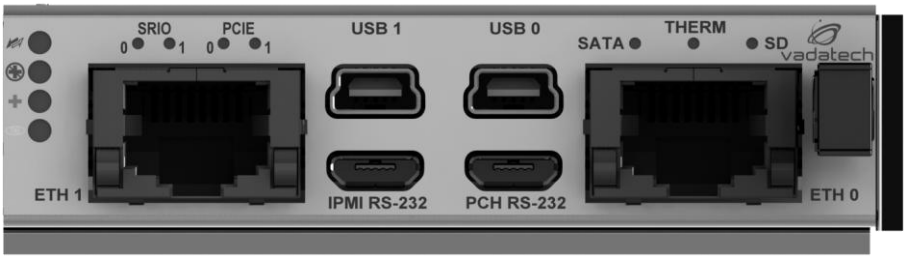

Figure 6: AMC722 Front Panel

Figure 7: AMC723 Front Panel

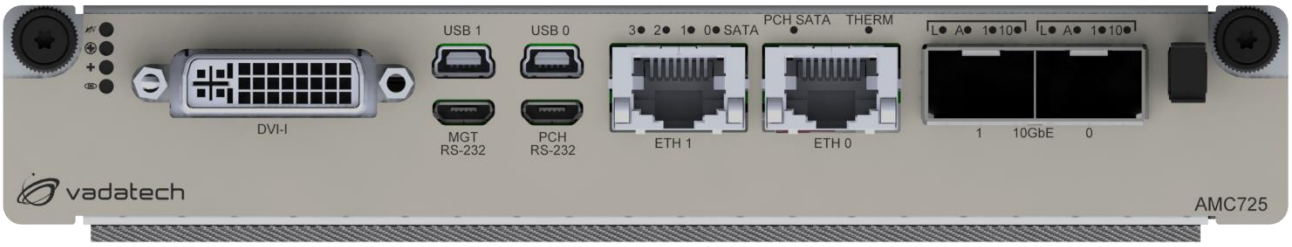

Figure 8: AMC725 Front Panel

Temperature Sensors

There are four temperature sensors on AMC72X boards. Figure 9 shows the location of temperature sensor on a typical AMC72X board.

Figure 9: Temperature Sensor Location (Bottom Side of AMC72X Board) (X=0, 1, 2, 3)

IPMI Management Interface

The AMC72X has an IPMI Module Management Controller (MMC) which manages the LEDs, module hot-swap handle, e-keying and port status, etc.

The behavior of the IPMI LEDs is as follows:

LED	OFF	ON	BLINK
Blue	Card active	OK to remove	Hot-swap/power transitioning
Red	No Fault	Payload Power Fault	N/A
Green	No management power	Management power OK Payload power OK	Management power OK Payload power not expected
Amber	Normal	Firmware upgrade	N/A

Table 3: AMC LED Behavior

NOTE: The card should only be removed from the chassis when the AMC Blue LED is solid ON.

To insert the card to the chassis, place the card into the carrier's guide rails and push on the front panel firmly until it is fully seated into the connector. If the card does not go fully in, do not force it and instead remove it and check for proper orientation or obstructions. Once fully inserted the Blue LED should go to solid ON while the Green LED should start blinking. Then push in the handle to latch the card into the carrier, the Blue LED should blink for a time and then go solid OFF while the Green LED goes solid ON.

To remove the card, pull out the hot-swap handle until it stops to unlatch the card from the carrier (but do not pull hard enough to remove the card itself yet). The Blue LED should blink for a time and then go solid ON. Once it does, pull the hot-swap handle straight out firmly to remove the card from the carrier.

The AMC72X also has an "IPMI RS-232" connector which enables a serial connection to the IPMI MMC CPU. A VadaTech serial cable assembly is available for connecting to this port which converts the Micro USB form factor into a DB9 connector (VadaTech P/N CBL-DB9MUSB1).

This port operates with 115200-8N1-NOFLOW settings, and the port is pinned out as follows:

Pin	Signal
1	Open
2	Receive
3	Transmit
4	Open
5	Signal GND
SHLD	Chassis GND

Table 4: IPMI RS232 connector pin-out

WARNING: Please take care not to plug USB devices into the "IPMI RS-232" port as there may be a risk of damage. Even though the connector accepts Micro-USB cables, this port is not electrically compatible with USB devices.

IPMI Internal 10/100 Ethernet

The MMC makes use of CaveCreek PCH Manageability Capability to configure Management Port over one of four 1GbE ports for SOL traffic. This Ethernet port is managed by the MMC and is not accessible to the customer directly. The customer can make use of it indirectly however by using the Serial Over LAN (SOL) functionality of the MMC.

Please refer to the VadaTech MMC and IPMC RMCP and SOL Guide.

Sensors

The AMC72x Management Controller monitors the following sensors:

Sensor #	Name	Description
0x90	VT AMC72x HS	AMC.0 Hot-Swap Sensor
0x10	VT AMC72x T1	Intake Air Temperature
0x11	VT AMC72x T2	Temperature near power section
0x12	VT AMC72x T3	Temperature near power section
0x13	VT AMC72x T4	Exhaust Air Temperature
0x20	VT AMC72x 12V	12V Input Power
0x30	VT AMC72x Tpch	PCH DIE temperature
0x31	VT AMC72x Tcpu	CPU DIE temperature
0x32	VT AMC72x Tdimm0	Dimm 0 temperature
0x33	VT AMC72x Tdimm1	Dimm 1 temperature
0x34	VT AMC72x wCPU	Power consumption in Watts
0x3D	VT BIOS POST	BIOS Post Code
0x3E	VT CPLD STATUS	CPLD status
0x3F	VT CPLD Version	CPLD HDL version

Table 5: MMC Sensors

To list the sensors, use this command:

```
# ipmitool sdr
```

DIP Switch Settings

The AMC72X products contain numerous DIP switches which will be pre-set by the factory. Some switch settings may need to be changed by the customer in order to match their desired configuration. Factory default settings are marked as blue.

1.1.1 IPMI Related functions

SW2[1:3] control IPMI related functions and are primarily intended for VadaTech use.

Switch	OFF	ON
SW2-1	Factory Default	Reserved
SW2-2	Factory Default	Reserved
SW2-3	Factory Default	Reserved

Table 6: SW2 settings

NOTE: Please do not change the factory default settings unless instructed by VadaTech.

1.1.2 Write Protection Switches

SW2[4] and SW3[1:2] control write protection of various programmable parts available on the board.

Switch	Description	OFF	ON
SW2-4	SD Card Write-Protect	Write-Protected	Writeable
SW3-1	SPI Flash 0 Write-Protect	Writeable	Write-Protected
SW3-2	SPI Flash 1 Write-Protect	Writeable	Write-Protected

Table 7: Write Protection Switch Settings

1.1.3 Board Configuration Switches

SW3[3:4] and SW4 control board relative features which are generic for all AMC72X boards.

Switch	Description	OFF	ON
SW3-3	Don't reboot system on second try.	Reboot After Second Timeout	No Reboot After Second Timeout
SW3-4	PCIe Ref Clock Source	On-Board Clock	Backplane Fabric Clock

SW4-1	RTC Reset	Normal State	Reset Asserted
SW4-2	Secondary RTC Reset	Normal State	Reset Asserted
SW4-3	7-Seg DisplayMode	Bios Post Code	Power State Mode
SW4-4	PCIe Port Bifurcation Strap	x8	Dual x4

Table 8: Board Configuration Switch Settings

Note: SW4-4 is available only on AMC720 and AMC725, since only these boards have PCIe on Ports 4-11 and can be configured as dual x4 or single x8 link. Refer to Section **IPMI E-Keying Configuration** for the steps to configure the module e-keying records for the respective configuration.

1.1.4 SRIO Configuration Switches

SW5 and SW6 are used to configure SRIO on AMC722 ports 4-7 and 8-11.

NOTE: Since both switch SW5 and SW6 settings have exactly the same meaning this section will cover switch configuration only for SW5 keeping in mind that SW6 has the same purpose and applies for second SRIO port.

Switch	Description	OFF	ON
SW5-1	Boot from EEPROM Strap	Disabled	Enabled
SW5-2	Boot from SRIO	After Software sets SRBOOT_CMPL bit	After Fundamental Reset
SW5-3	SRIO Host/Slave Control	SRIO Slave	SRIO Host
SW5-8	Reserved	Factory Default	Reserved

Table 9: SRIO Configuration Switch Settings

SW5[3:4]	Result
ON-ON	BASE_ID = 0xFE LAR_BASE_ID = 0x00FE
ON-OFF	BASE_ID = All Ones LAR_BASE_ID = All Ones

Table 10: SRIO Base Device ID Control Switch Settings

SW5[5:7]	Result
OFF-OFF-OFF	5.0Gbaud
OFF-OFF-ON	2.5Gbaud
OFF-ON-OFF	1.25Gbaud
ON-OFF-ON	3.125Gbaud

Table 11: SRIO Speed Settings

Gladden Interface

Serial Console Port

The AMC72X front panel includes a "CPU RS-232" connector which enables a serial console connection to the CPU using Serial Port 0 exported by CaveCreek PCH. Output redirection to the serial port is configured using BIOS configuration menu. A VadaTech serial cable assembly is available for connecting to this port which converts the Micro USB form factor into a DB9 connector (VadaTech P/N CBL-DB9MUSB1).

This port operates with 9600-8N1-NOFLOW settings; the port is pinned as follows:

Pin	Signal
1	Open
2	Receive
3	Transmit
4	Open
5	Signal GND
SHLD	Chassis GND

Table 12: CPU RS232 connector pin-out

WARNING: Please take care not to plug USB devices into the "CPU RS-232" port as there may be a risk of damage. Even though the connector accepts Micro-USB cables, this port is not electrically compatible with USB devices.

NOTE: This RS-232 port is not available during the time that a Serial Over LAN (SOL) session is active to the board using Serial Port 0 since during that time the Serial Port 0 is automatically switched away from the front panel and is connected to the MMC so that it can convey the serial traffic via Ethernet.

USB Ports

The AMC72X front panel includes two USB ports. USB Ports are connected to the CaveCreek USB Ports 0 and 1. A USB device may be attached to this port for expansion.

Pin	Signal
1	+5V
2	D-
3	D+
4	Open
5	Signal GND
SHLD	Chassis GND

Table 13: USB port pin-out

1GbE Ports

There are two 10/100/1000Base-T (copper) Ethernet ports available on the front panel. ETH0 and ETH1 are attached to the CaveCreek 1GbE ports 2 and 3 via two 88E1114 PHYs.

Dedicated 1000Base-X Ports are connected to CaveCreek 1GbE Ports 0 and 1 and then to AMC Ports 0 and 1.

The LEDs on the RJ45 ports on the front panel replicate the state of four 1Gbe ports exported by CaveCreek. The LEDs for those ports are defined as follows:

LED	ON	OFF	BLINK
Green	GbE2 Linked	GbE2 not linked	GbE2 Activity
Orange	GbE0 linked	GbE0 not linked	GbE0 Activity

Table 14: ETH0 LEDs

LED	ON	OFF	BLINK
Green	GbE3 Linked	GbE3 not linked	GbE3 Activity
Orange	GbE1 linked	GbE1 not linked	GbE1 Activity

Table 15: ETH1 LEDs

XAUI Ports (only applicable to AMC721 and AMC723)

Depending on the board model, there are up to two available XAUI ports on the backplane. AMC721 provides XAUI ports on AMC 4-7 and AMC 8-11, while AMC723 only provides a single XAUI port on AMC 8-11.

The LEDs on the front panel on both of these AMC modules provide indication of Link and Activity for the available ports per the following table:

LED	ON	OFF	BLINK
A	n/a	No activity	Activity
L	Corresponding port linked	Corresponding port not linked	n/a

Table 16: 10GbE LEDs

SRIO Ports (only applicable to AMC722)

AMC722 provides dual SRIO x4 interface on backplane lanes 4-7 and 8-11. Since the SRIO interface is available via a PCIe-to-SRIO Bridge, front panel LEDs reflect the current state of both sides of the bridge, hence the SRIO and PCIE LEDs above ETH 1 connector.

Such LEDs are defined as follows:

LED	ON	OFF	BLINK
SRIO 0/1	Corresponding SRIO port detected reset	Normal Function	n/a
PCIE 0/1	Corresponding PCIe port detected Hot Reset	Normal Function	n/a

Table 17: SRIO Bridge LEDs

SD Card Socket

The AMC72X board includes a Micro SD card socket. This socket connects to the Gladden by way of a USB2244 USB SD media controller chip. This SD card is typically used to hold the kernel and root file-system. This socket has a front panel LED associated with it as follows:

LED	Color	ON	OFF	BLINK
SD	Green	n/a	No activity	Activity

Table 18: SD Card LED

CaveCreek EEPROM

An AT25128B EEPROM is provided on the CaveCreek EEPROM port. This EEPROM is delivered with factory programmed image which contains default PCIe configuration space and CaveCreek GbE register settings. This EEPROM can be customized using Intel EEPROM Image Creation Tool (EICT). To flash the EEPROM image use Intel eepdate tool.

DDR3 SO-DIMMs

The board comes pre-loaded with either 4GB, 8GB, or 16GB of DDR3 memory with ECC depending on ordering option "B". The memory is carried on VadaTech proprietary SO-DIMMs and inserted in slots J2 and J3 on the board. The software uses the SO-DIMM's SPD EEPROMs to determine the size and type of memory.

Slot	Chip Select	Data Width	TWSI0 SPD EEPROM
J2	*DDR_DIMM0_CS0	64-bit + 8-bit ECC	"1010010"
	*DDR_DIMM0_CS1		
J3	*DDR_DIMM1_CS0		"1010001"
	*DDR_DIMM1_CS1		

Table 19: DDR3 SO-DIMM mapping

Ethernet PHY Addressing

The AMC72X board includes two 1GbE PHYs.

PHY Address	Type	Port
0x01	88E1114	1GbE ETH0
0x02	88E1114	1GbE ETH1

Table 20: Gladden Ethernet PHY Addressing

NOTE: The backplane 1GbE ports and XAUI ports (if applicable) do not have a PHY; 1GbE ports are connected from CaveCreek PCH chip to the backplane without going through a PHY.

Software

The AMC72x comes pre-configured with AMI Aptio BIOS installed in the SPI flash devices, and Fedora installed in the on-board micro SD card.

BIOS

The BIOS is AMI Aptio version 4.6.5.4; it is based on the Intel Stargo Customer Reference Board with modifications to support the AMC72x hardware.

Setup Menu

After a power cycle or reset, the BIOS will present a welcome screen via the PCH serial port. Pressing the Del key causes the Setup Menu to be displayed. From Setup the customer may modify the BIOS settings as needed; for example the Boot menu is used to modify the boot device order.

Updating the BIOS

The Intel Flash Programming Tool, FPT is used to re-flash the BIOS firmware. Another option is to use the AMI AFU utility to re-flash the BIOS with a new image. Versions for DOS, Windows, and EFI are available from Vadatech on following link.

```
http://www.vadatech.com/amc72x/files/BIOS/
username: customer
password: amc72xvt@72
```

Here are the steps on how to re-flash BIOS using AMI AFU tool:

1. Download AMI AFU utility from the link above and extract on host PC
2. Go to `Aptio/afuefi`
3. Go to `32` or `64` depending on CPU
4. Open the archive file and copy .efi file to USB Flash Disk
5. Download BIOS upgrade image from the link above and extract to USB Flash Disk.
6. Disconnect USB Flash from host PC and connect to AMC72X
7. Select EFI shell from BIOS boot menu and boot to EFI
8. USB Flash should show up as `fs0`
9. Enter `fs0:` command to open USB Flash
10. Use following command to upgrade bios:
    `<efi_file_name.efi> <amc72x_u23_spi1_flash.CAP> /B /P /N /K`
11. After upgrade is done, power cycle the board

Network Boot (PXE)

To enable booting via the network (PXE boot) following steps should be performed:

1. Enter BIOS
2. Go to Advanced/Network Stack
3. Enable Network stack and make sure that Ipv4 PXE Support and Ipv6 PXE Support are enabled
4. Save changes and exit
5. Power cycle the board and enter BIOS
6. Go to Boot menu
7. Enter CSM Parameters submenu
8. Set Launch PXE OpROM poli to [Legacy first]
9. Save changes and exit
10. Power cycle the board and enter BIOS
11. Go to Boot menu
12. If your NBP (Network Bootstrap Program) does not support UEFI and Legacy mode is preferred then perform following steps

    a) Go to Network Device BBS Priorities
    b) You should see following devices
    IBA GE Slot 0101 v1350 (AMC port 0)
    IBA GE Slot 0102 v1350 (AMC port 1)
    IBA GE Slot 0103 v1350 (Front port 0)
    IBA GE Slot 0104 v1350 (Front port 1)

    c) Set Boot Option #1 the device which is connected to the network which has PXE server
    d) Exit submenu

13. Under Boot Option Priorities choose IBA GE Slot 010X v1350 if preferred to use legacy mode, or one of UEFI devices below, depending on which port is connected to the network with PXE server

    UEFI: IP4 Intel(R) DH8900CC Series Gigabit Backplane Network Connection (AMC port 0)
    UEFI: IP6 Intel(R) DH8900CC Series Gigabit Backplane Network Connection (AMC port 0)
    UEFI: IP4 Intel(R) DH8900CC Series Gigabit Backplane Network Connection (AMC port 1)
    UEFI: IP6 Intel(R) DH8900CC Series Gigabit Backplane Network Connection (AMC port 1)
    UEFI: IP4 Intel(R) DH8900CC Series Gigabit Network Connection (Front port 0)
    UEFI: IP6 Intel(R) DH8900CC Series Gigabit Network Connection (Front port 0)
    UEFI: IP4 Intel(R) DH8900CC Series Gigabit Network Connection (Front port 1)
    UEFI: IP6 Intel(R) DH8900CC Series Gigabit Network Connection (Front port 1)

14. Save changes and exit

After reboot AMC72X will try to locate PXE server and try to boot from it if present.

Boot Devices

To modify the boot device order, select the Boot tab and scroll down to Boot Option Priorities. Select the Boot Option number and change it by selecting from the list in the dialog box.

Watchdog

The AMC72x comes with watchdog feature which used to prevent the board from hanging after powering the board on different stages of booting process. The BIOS watchdog configuration page under BIOS setup Advanced->Watchdog menu is used to configure watchdog from BIOS. See the Figure 10 and Figure 11.
The AMC72X Watchdog feature allows to configure 3 type of watchdogs.

1. Watchdog 2 – Used to restart or power off the AMC72x payload when BIOS bank is corrupted.
2. Watchdog 3 – Used to restart or power off the AMC72x payload when BIOS POST (Power-On-Self-Test) failed.
3. Watchdog 4 – Used to monitor OS boot process.

All these watchdogs are independent and can be used separately.

BIOS Watchdog configuration

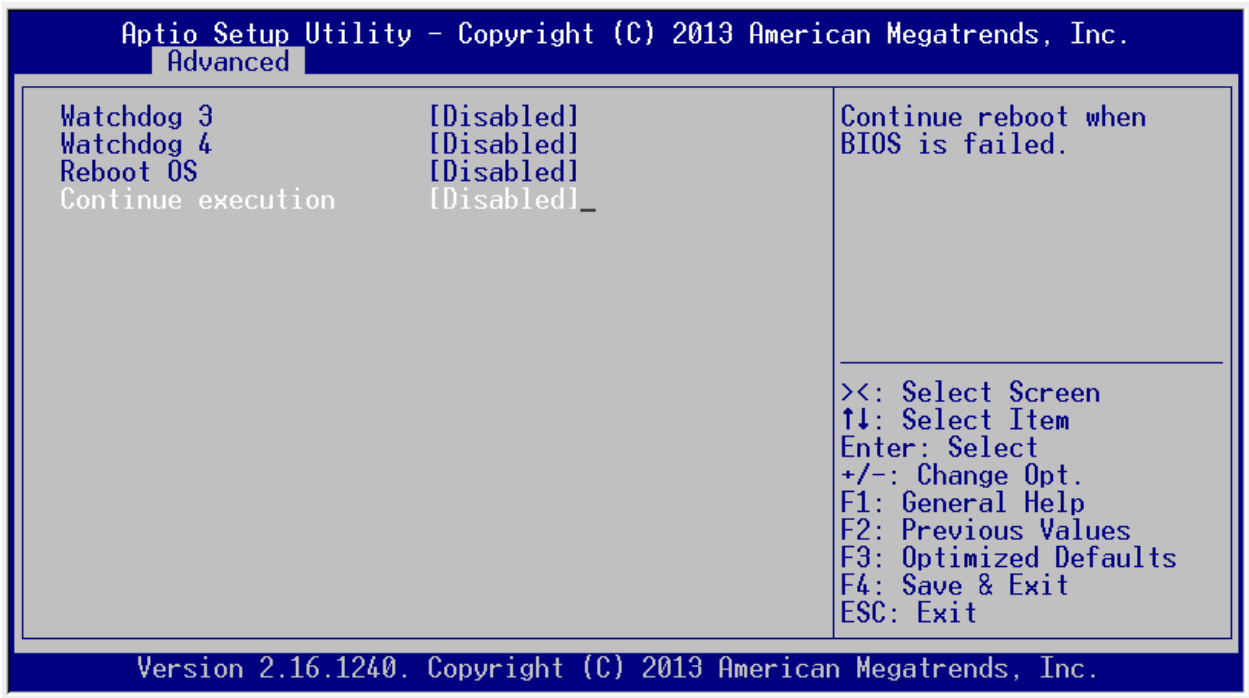

Figure 10: BIOS watchdog configuration page with default settings

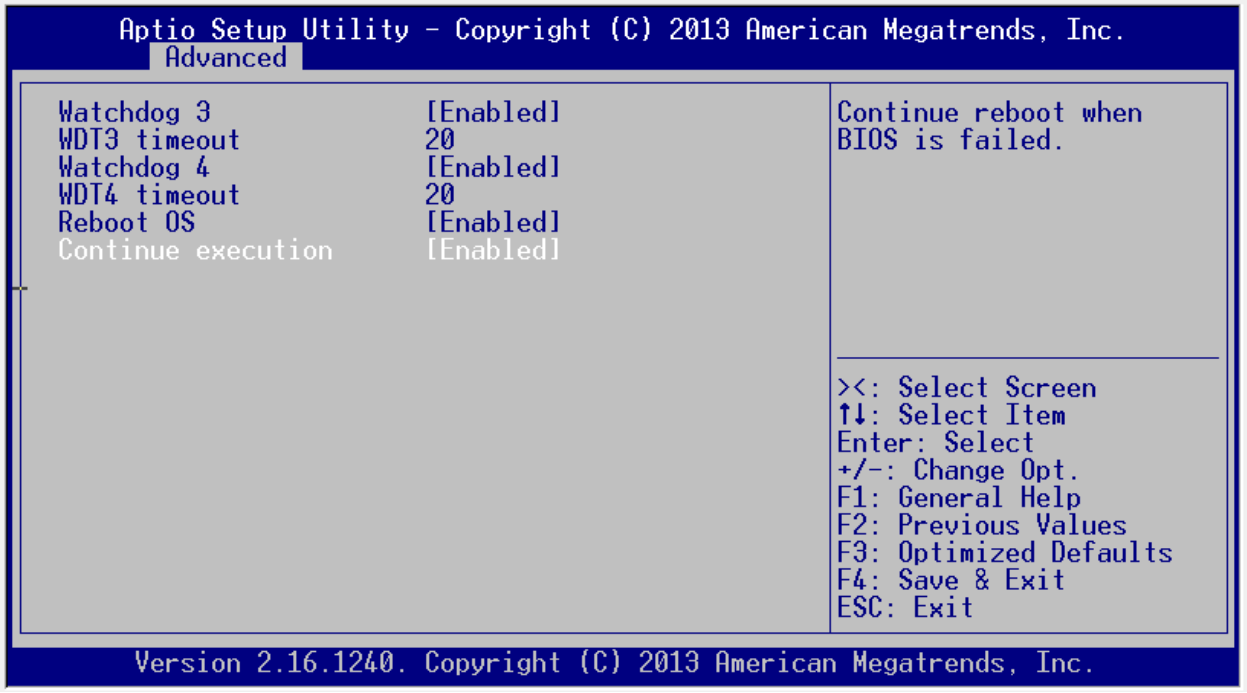

Figure 11: BIOS watchdog configuration page with all features enabled settings

The "Watchdog 3" setting is used to continuously restart or power off the AMC72x payload if BIOS does not reached POST OK stage within watchdog 3 provided timeout. To enable this feature necessary to enable "Watchdog 3" from menu then set Watchdog 3 timeout value in "WD3 timeout" tab. The WDT3 timeout configured in 15 seconds steps, minimum = 1 (15 sec), maximum = 31 (465 sec) and default is 20 (300 sec). The BIOS POST OK event stops the Watchdog 3. The "Watchdog 3" Disabled setting used to disable watchdog 3 functionality. To apply this setting BIOS configuration save and board power cycle is required. The default value for this setting is "Disabled". See the Figure 11 for "Watchdog 3" setting configuration from BIOS menu.

The "Watchdog 4" setting is used to continuously restart or power off the AMC72x payload if Operation System hangs during boot process. To enable this feature necessary to enable "Watchdog 4" from menu then set Watchdog 4 timeout value in "WD4 timeout" tab. The WDT4 timeout configured in 15 seconds steps, minimum = 1 (15 sec), maximum = 31 (465 sec) and default is 20 (300 sec). With enabled WDT4 the Operation System must stop "Watchdog 4" timer by setting "OS booting" bit to 1. "OS booting" bit is bit 7 of CPLD watchdog control byte2 which is mapped by BIOS on 0xCAB base address in ACPI address space. To apply this setting BIOS configuration save and board power cycle is required. The default value for this setting is "Disabled". See the Figure 11 for "Watchdog 4" setting configuration from BIOS menu.

The "Reboot OS" setting is used to continuously restart the board when Watchdog 4 timeout is reached and "OS booting" bit does not set by Operation System. When this setting is disabled then in case of Watchdog 4 timeout board will be powered off. The default value for this setting is "Disabled". See the Figure 11 for "Reboot OS" setting configuration from BIOS menu.

The "Continue execution" setting is used to continuously restart the board after 30 second in case when BIOS boot does not start. When this setting is disabled the board will be powered off if BIOS does not start during 30 second. The default value for this setting is "Disabled". See the Figure 11 for "Continue execution" setting configuration from BIOS menu.

The BIOS menu "Save", "Restore" and other options used to store/restore/reset the BIOS settings applies on Watchdog configuration accordingly.

MMC watchdog configuration

The MMC CLI provides interface for watchdog pre boot settings configuration.
The MMC CLI main menu "wdcfg" command is used to enter cli into watchdog configuration mode. See Figure 12.

```
> wdcfg

Watchdog Configuration:
  WD2 state           : Enabled
  Continue Execution  : Enabled

Commands:
  set wd2 <on|off>         - Enable/Disable WD2
  set contexec <on|off>    - Enable/Disable Continue Execution
  show                     - Show current configuration
  done                     - Return to Main CLI
>
```

Figure 12: MMC CLI watchdog configuration mode

The "set wd2 <on|off>" command used to on/off watchdog 2 timer which is used to reboot or power off the payload when BIOS is corrupted. The factory default is "off".
The "set contexec <on|off>" command used to enable payload reboot when watchdog 2 timer is elapsed. The factory default is "off".
The "show" commands prints the current configured settings and commands list.
The "done" commands leaves the watchdog configuration mode and returns to MMC CLI main.

On change all these commands settings stores as permanent.

Linux

The AMC72x comes pre-programmed with Fedora installed in the on-board SD card. Linux includes many different commands and features, which cannot all be described here. Additional documentation resources can be found on-line at fedoraproject.org and on other Linux resource site.

Logging In

The PCH serial port is used to log-in to Linux using the 9600 8N1 settings. At the log-in prompt you should see the following:

```
Fedora release 18 (Spherical Cow)
Kernel 3.9.4-200.fc18.x86_64-vt on an x86_64 (/dev/ttyS0)

localhost login: root
Password: rootroot
```

Log-in as root using the password as shown above. You may change the root password after logging-in.

Network Device Mapping

The AMC72x family devices have four 4 GbE interfaces 2 of them routed to front Ethernet ports, two of them routed to AMC Ports 0 and 1. XAUI ports are present on AMC Ports 4-7 and 8-11 depending on particular product. For more information refer to tables below.

Interface	Default IP Address	Type	Port
ge0	192.168.40.212	GbE	AMC Port 0
ge1	192.168.41.212	GbE	AMC Port 1
ge2	192.168.1.199	GbE	ETH 0
ge3	192.168.2.199	GbE	ETH 1

Table 21: AMC720 and AMC722 Network Device Mapping

Interface	Default IP Address	Type	Port
xe0	192.168.42.212	XAUI	AMC Ports 4-7
xe1	192.168.43.212	XAUI	AMC Ports 8-11
ge0	192.168.40.212	GbE	AMC Port 0
ge1	192.168.41.212	GbE	AMC Port 1
ge2	192.168.1.199	GbE	ETH 0
ge3	192.168.2.199	GbE	ETH 1

Table 22: AMC721 Network Device Mapping

Interface	Default IP Address	Type	Port
xe0	192.168.42.212	XAUI	AMC Ports 8-11
xe1	N/A	N/A	Not Connected
ge0	192.168.40.212	GbE	AMC Port 0
ge1	192.168.41.212	GbE	AMC Port 1
ge2	192.168.1.199	GbE	ETH 0
ge3	192.168.2.199	GbE	ETH 1

Table 23: AMC723 Network Device Mapping

NOTE: Only first 10GbE port is connected to AMC Ports. Second port is unconnected and shows up as a dummy port in Linux. It cannot be used.

Interface	Default IP Address	Type	Port
xe0	192.168.42.212	XAUI	10Gbe 0
xe1	192.168.43.212	XAUI	10Gbe 1
ge0	192.168.40.212	GbE	AMC Port 0
ge1	192.168.41.212	GbE	AMC Port 1
ge2	192.168.1.199	GbE	ETH 0
ge3	192.168.2.199	GbE	ETH 1

Table 24: AMC725 Network Device Mapping

Auto-negotiation Capability

Starting from release 8 all AMC72x family GbE interfaces are capable to disable auto-negotiation through "ethtool" and forcibly set duplex and speed. The command below will disable Auto-negotiation on ge0 interface and set speed and duplex to 1GbE full duplex:

```
# ethtool -s ge0 autoneg off speed 1000 duplex full
```

VNC Server

The Linux GUI can be accessed remotely over the network since there is a VNC server installed in the Linux. The server is preconfigured and ready to use, but it is off by default. Use the command bellow to start VNC server:

```
# vncserver :1 -geometry 800x600 -depth 24
```

The following command stops VNC server:

```
# vncserver -kill :1
```

The password for VNC server is same as password for root user.

BSP Version

bsp-version command shows current BSP release number. Also it shows the kernel release and the kernel version.

Note: Payload BSP allocates 16GB disk space. You can mount and use the remaining disk space. Refer to the product ordering option for available disk space.

Graceful Shutdown Support

Graceful shutdown provides a way of gracefully shutting down the OS running on the board once payload deactivation request from uTCA Carrier is received due to explicit deactivation command or AMC handle opened.

Graceful shutdown a result of cooperation of different components of AMC design which are described below:

1. Module Management Controller supports
    a. OEM IPMI commands which allow the user to enable/disable graceful shutdown support and configure maximum delay that MMC waits for the payload shutdown
    b. Read the Quiesced state of the AMC to determine whether AMC deactivation has been requested by uTCA Carrier Manager
    c. Monitor of CPU power state to detect system shutdown completion
2. Hardware support
    a. LPC interface between MMC and Payload CPU.
3. Application running on OS side
    a. Performs AMC Quiesced state monitoring through LPC interface using OEM IPMI commands and gracefully shuts down the OS once deactivation is requested by uTCA Carrier Manager.

NOTE: OS side Graceful shutdown support is OS specific and the user should implement its own way of shutting down the board using provided interface and OEM IPMI commands. Vadatech has the Graceful shutdown support in place for Fedora Linux available on SD Card shipped with the board.

1.1.5 Implementing Graceful Shutdown

In order to implement graceful shutdown support in the OS following stuff is required:

1. Driver to be able to communicate on payload LPC bus
2. Interface for sending IPMI packets over LPC bus

IMPORTANT: Default Linux implementations support ipmi_si driver which is part of ipmitool project and is compatible with the VadaTech Module Management Controller.

Following arguments should be passed to the driver to make it communicate with the MMC through the LPC bus:

```
ports=0xca2 regspacings=4
```

By default MMC is initialized with graceful shutdown support disabled allowing proper operation of operating systems which do not implement graceful shutdown.

After OS starts graceful shutdown support should be enabled by the software using IPMI "Set Graceful Shutdown" OEM command. This command also supports optional *payload shutdown delay* parameter (two bytes). This specifies the maximum delay that MMC waits for the payload shutdown,

After enabling graceful shutdown the software should continuously monitor Quiesced state of the AMC by issuing IPMI "Get Quiesced State" OEM command.

Once AMC goes to "Quiesce In Progress" state the software should start OS shutdown. MMC will monitor payload power state and report that payload has been turned off to uTCA carrier once CPU goes to power down state. If the payload doesn't shutdown within the specified period (*payload shutdown delay*) then MMC switch Quiesced state.

Name	NetFn	Cmd	Input Data	Output Data
Set Graceful Shutdown	0x2e	0x37	byte[0] = 0x32 byte[1] = 0x5d byte[2] = 0x00 byte[3] = *value* (byte[4] = *payload shutdown delay high byte* byte[5] = *payload shutdown delay low byte)* *value*: 0 - Disable 1 - Enable *Payload shutdown delay high/low bytes*: Delay on seconds	byte[0] = IPMI CompCode byte[1] = 0x32 byte[2] = 0x5d byte[3] = 0x00
Get Quiesced State	0x2e	0x38	byte[0] = 0x32 byte[1] = 0x5d byte[2] = 0x00	byte[0] = IPMI CompCode byte[1] = 0x32 byte[2] = 0x5d byte[3] = 0x00 byte[4] = *value* *value*: 0 - Not Quiesced 1 - Quiesce in Progress 2 - Quiesced

Table 25: Graceful Shutdown IPMI OEM Commands

CPU state monitoring and AMC deactivation

The MMC on AMC72x boards is consistently monitoring the power state of the CPU and is able to detect when OS shutdown command is executed from payload and CPU goes into power off state.

Once the power off is detected by MMC or the *payload shutdown delay* is expired it will deactivate the AMC and board will go into M1 state allowing the MCH to reactivate the board.

IPMI E-Keying Configuration

An AMC E-Keying menu is available via the IPMI RS-232 port for AMC720 and AMC722. This e-keying configuration is already performed at the factory to match the ordering options of the board. However, this menu can be accessed if desired to turn on/off sets of backplane e-keying records for the GbE, PCIe, SRIO and SATA ports.

To use the menu system simply follow the on-screen directions to enable/disable the various sets of e-keying records. When a set of records is enabled it will have an asterisk next to it and when it is disabled it will not have the asterisk.

After configuring e-keying please remove and reinsert the card to ensure that the carrier manager correctly re-reads the contents of the e-keying records.

Following tables map switch settings to suggested e-keying configuration.

SW4-4	Active E-Keying options	Result
OFF	1, 2, 3, 5, 6, 7	PCIe x8
ON	1, 2, 3, 4, 6, 7	PCIe Dual x4

Table 26: AMC720 E-Keying Configuration

SW5[5:7]	Active E-Keying options	Result
OFF-OFF-OFF	1, 2, 3, 7, 11, 12	5.0Gbaud
OFF-OFF-ON	1, 2, 5, 9, 11, 12	2.5Gbaud
OFF-ON-OFF	1, 2, 6, 10, 11, 12	1.25Gbaud
ON-OFF-ON	1, 2, 4, 8, 11, 12	3.125Gbaud

Table 27: AMC722 E-Keying Configuration

Serial Over Lan (SOL)

The Serial Over Lan function can redirect the CPU RS-232 serial ports into an SOL network session. When using `serial0` as SOL serial port software will redirect the port from front panel to SOL session. This allows for straightforward remote access to the CPU console serial port without the need for having an RS-232 cable connected to the serial port.

CaveCreek exports two serial ports (`serial0` and `serial1`). Configuration command is available on IPMI RS-232 port to select serial port for SOL using `plser` command.
One of four 1GbE ports can be configured as a management port to direct SOL traffic. This option is software configurable and can be modified using `mgtport` command to select one of two backplane ports (`back0` and `back1`) or one of two front panel ports (`front0` and `front1`) as management port.

A separate manual is available describing additional functionality. Please refer to the VadaTech MMC and IPMC RMCP and SOL Guide.

Factory Setup

Initial Factory Setup

The MAC addresses for the board should already be configured by VadaTech during manufacturing. Take care not to erase CaveCreek EEPROM so as not to lose the globally unique MAC addresses that have been assigned.

In the factory these MAC addresses are assigned as follows:

1) TARGET: Boot DOS using bootable USB Flash Stick
2) PC: Reserve 5 MAC addresses from the VadaTech MAC pool for each 1Gbe ports plus 1 port for IPMI/SOL Management traffic
3) TARGET: Use **`eeupdate`** tool to set MAC addresses.

NOTE: Management port will automatically assign itself 5th reserved MAC address.

NOTE: The board must be power-cycled or reset after setting the MAC address before it will take effect.

For AMC721 and AMC723 same steps should be performed to update MAC addresses on XAUI ports.

Writing the Factory Default Payload BSP

An image is provided in the BSP release package to restore the default Payload BSP.

Payload BSP is restored/flashed with Clonezilla software. Clonezilla is a free partition and disk imaging/cloning program. Clonezilla live allows you to use USB flash drive to boot and run clonezilla. To install Clonezilla live, the basic steps are

1. Clonezilla Live **zip** package and **Tuxboot** application are available from Vadatech on following link:

```
http://www.vadatech.com/amc72x/files/Clonezilla/
username: customer
password: amc72xvt@72
```

2. Run the **Tuxboot** application. Check **Pre Downloaded** radio button and select the image zip file downloaded by step #1. Select the USB drive to install Clonezilla Live on your USB flash drive (DISK1).

These steps describe target disk flashing process.

1. Extract BSP image file and copy to USB disk (DISK2) which will serve as a source to flash target disk contents.
2. Connect both DISK1 and DISK2 to AMC72x and boot Clonezilla from DISK1. Make sure that BIOS boot option for DISK1 is in legacy mode. From Clonezilla boot menu select **Clonezilla Live (Serial Console)** boot option.
3. You should not change most of default settings when use Clonezilla setup. Choose **device-image** mode and assign where the Clonezilla image will be read from (**local_dev**).
4. After using local device you need to mount a DISK2 so that you can read the image. Choose **restoredisk** option and the image file to restore an image to local disk.
5. Choose the target disk to be overwritten.

Expect the copying process to take around 10-15 minutes.

AMC725 Specific Changes

The AMC725 is the latest in AMC72x series of Processor AMCs. This section describes the key differences between the AMC725 from AMC720, 1, 2, and 3.

Block Diagram

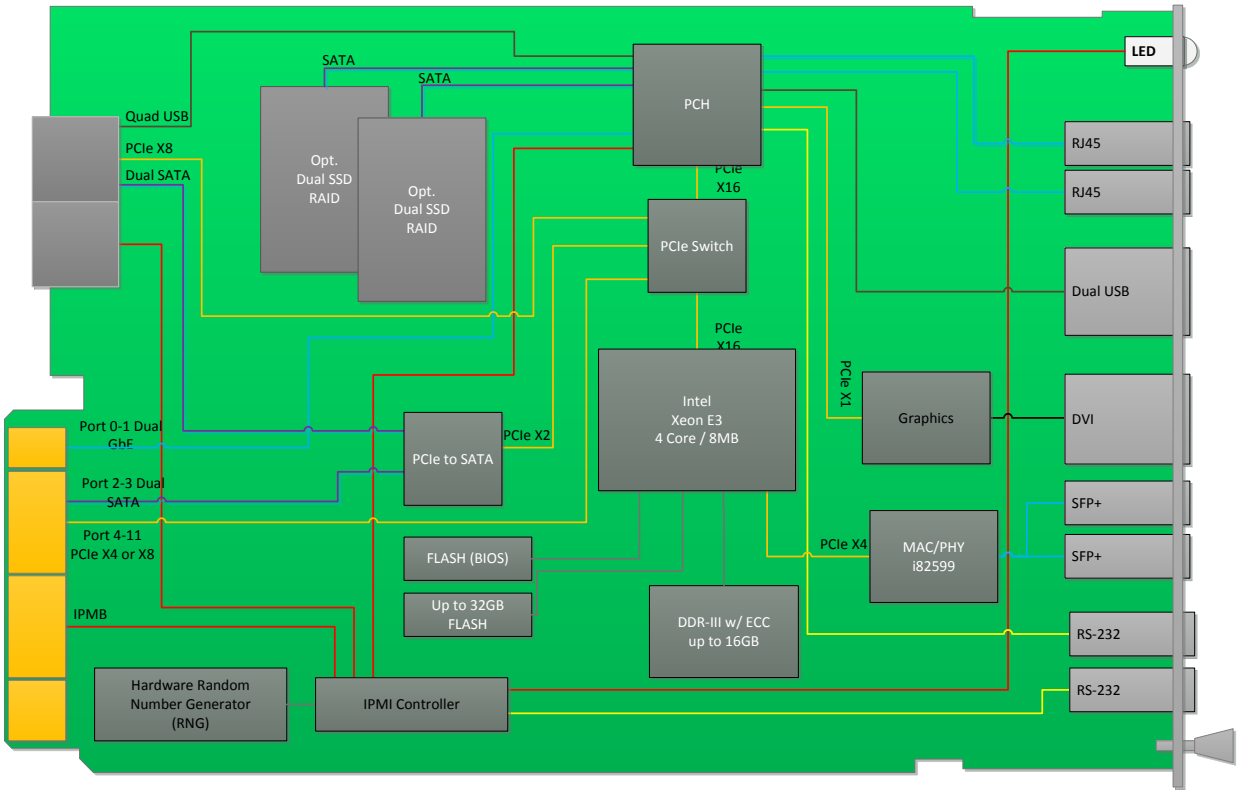

Figure 13: AMC725 Block Diagram

Summary

The summary of key differences in AMC725 compared to the other AMC72x devices are:

- AMC725 is a double-width, mid-height Advanced Mezzanine Card, with options for full-height.
- AMC725 has a built-in graphics controller, routed to the front panel through the DVI-I connector
- Support for two SATA disk drives (one on the baseboard and other on an optional daughter board)

- AMC725 supports additional peripherals and interfaces compared to other AMC72x device and to support these additional features a PCIe Gen 3 switch is used
- Ports 4 to 11 on AMC725 are routed from the PCIe Gen 3 switch to the backplane connectors
- From the PCIe Gen3 Switch:
    - PCIe x16 to PCH
    - PCIe x16 to CPU
    - PCIe x8 to RTM connector
    - PCIe x1 to Graphics controller
    - PCIe x2 to SATA controller, which controls the Ports 2 and 3
- The 10GbE NIC on AMC725 is routed to the front panel through dual SFP+ connectors
- µRTM Connector provides the following interfaces:
    - 4x USB from PCH
    - PCIe x8 from PCIe Gen3 Switch
    - 2x SATA ports
    - 2x PCIe reference clocks

Switches and Sensors

The location on switches and temperature sensors on AMC725 are shown below.

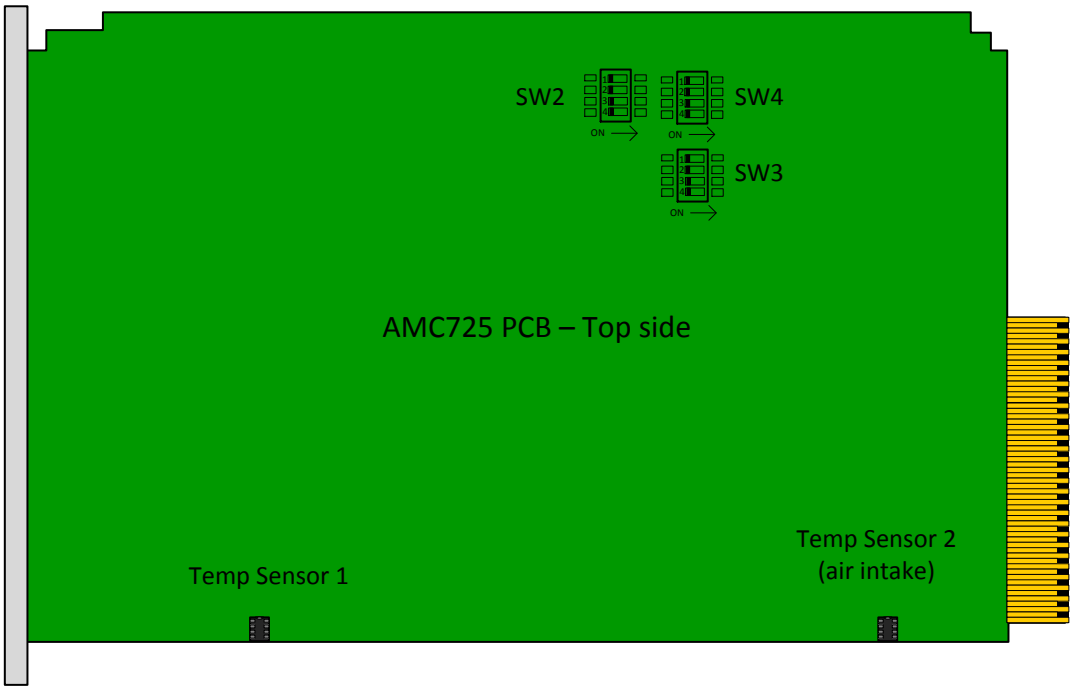

Figure 14: AMC725 PCB Top Side

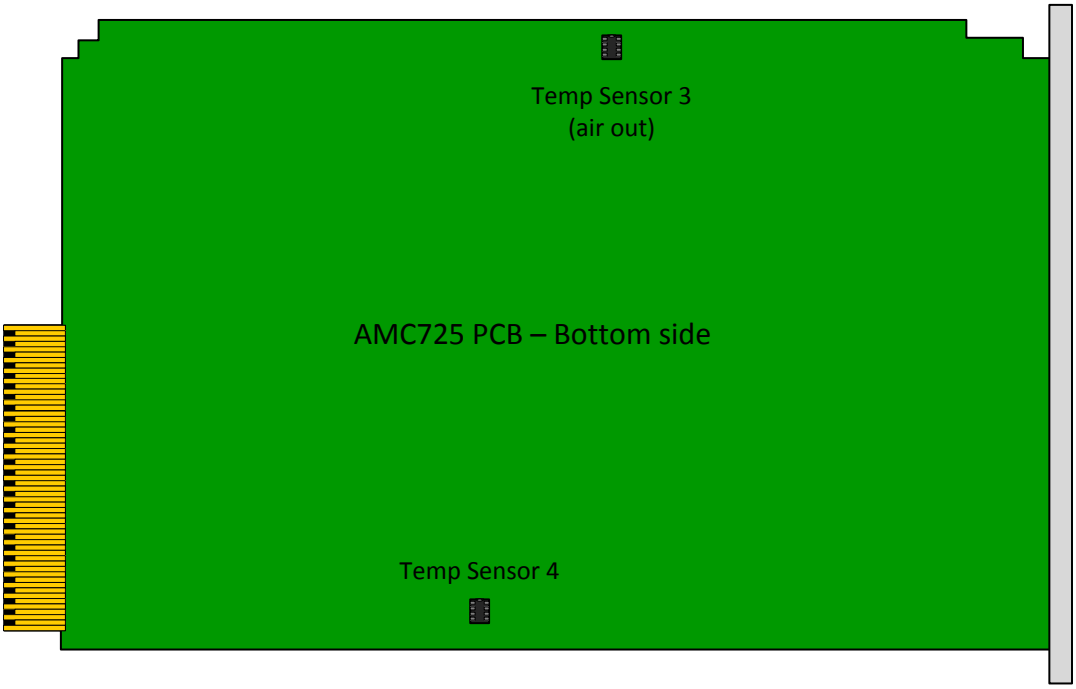

Figure 15: AMC725 PCB Bottom Side

Recommended Sanitizing Procedures

This section describes the recommended approach for handling AMC72x when entering/leaving a secure environment. Some customers of VadaTech will need to have assurance when taking AMC72x from a secure environment that the contents of the nonvolatile memories are either erased, in a 'factory default' state, or in some other way are assured to not contain classified information of any kind. This is especially true if a product requires factory service.

This section describes the non-volatile memory components on the AMC72x board and the approach that VadaTech feels is the most reasonable way to manage sanitizing them without adversely affecting the product's ability to still function.

VadaTech does not guarantee that these procedures will comply with any specific company's or government's security policies. Therefore, please review your particular security requirements carefully and compare them to this document to ensure that you remain in compliance with the requirements. If you have any questions please contact VadaTech technical support at support_team@vadatech.com.

Sanitizing: BIOS and OS

The following procedure will sanitize the Bios (programmed on SPI device) and Operating System (installed on SD card).

For programming BIOS with factory default image refer to Updating the BIOS section.

For installing factory default Fedora Operating System refer to Writing the Factory Default Payload BSP section.