VadaTech AMC502

Hardware Reference Manual

April 30, 2015

Version 1.1.0

vadatech inc

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Revision History

Doc Rev	Description of Change	Revision Date
1.0.0	Document created	3/6/2015
1.1.0	Corrected FPGA banking/floorplan diagrams.	4/30/2015

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Figures

Tables

1 Document Overview

This document describes the AMC502 board hardware. The AMC502 is an FMC carrier FPGA board which hosts a Xilinx Kintex-7 FPGA and two FMC sites.

1.1 Applicable Products

- VadaTech AMC502 (Kintex-7)

1.2 Document References

- VadaTech AMC502 Datasheet (http://www.vadatech.com)
- VadaTech FMCs User Manual
- PICMG® AMC.0 AdvancedMC Mezzanine Module (http://www.picmg.org)
- PICMG® AMC.1 AdvancedMC PCI Express and AS (http://www.picmg.org)
- PICMG® AMC.2 AdvancedMC Ethernet (http://www.picmg.org)
- PICMG® AMC.4 AdvancedMC Serial RapidIO (http://www.picmg.org)
- Xilinx Kintex-7 Datasheets and User's Guides
- ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard (http://www.vita.com)

1.3 Acronyms Used in this Document

Acronym	Description
AMC	Advanced Mezzanine Card
C2M	Carrier-to-Mezzanine (signal)
CGND	Chassis Ground
CLK	Clock
CPU	Central Processing Unit
DDR3	Dual Data Rate 3 SDRAM
DIP	Dual In-line Package
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FRU	Field Replaceable Unit
GbE	Gigabit Ethernet
GND	Signal Ground
HPC	High Pin Count (FMC connector)
IP	Intellectual Property
IPMI	Intelligent Platform Management Interface
JSM	JTAG Switch Module
JTAG	Joint Test Action Group

LED	Light Emitting Diode
LPC	Low Pin Count (FMC connector)
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signaling
M2C	Mezzanine-to-Carrier (signal)
MB	Megabyte (2^20 bytes)
M-LVDS	Multi-point Low Voltage Differential Signaling
MMC	Module Management Controller (IPMI controller of AMC)
n.c.	No connection
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PHY	Physical Layer Device
PICMG	PCI Industrial Computer Manufacturer's Group
PLL	Phase Locked Loop
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer/Deserializer
SRIO	Serial RapidIO
SSIF	SMBus System Interface
TCLK	Telephony Clock
VADJ	Adjustable Voltage (power rail)
VIO	I/O Voltage (power rail)
VREF	Reference Voltage (power rail)
XAUI	10GbE Attachment Unit Interface

Table 1: Acronyms

2 Hardware Overview

The AMC502 is a dual FMC carrier card with on-board FPGA in an AMC form-factor. It includes the following primary components (your ordering option may vary):

- Xilinx Kintex XC7K420T FPGA in FFG1156 package
    - 64MB QSPI Configuration/User Flash (S25FL512S or equivalent)
        - QSPI flash mux controlled by iMX6 CPU for field upgrade via Ethernet
    - Dual M-LVDS Crossbar Switches (IDT8V54816) for Backplane/FMCs/QPLL
    - Quad PLL (ZL30162) for clock jitter cleaning/frequency synthesis
    - 12 lanes of SERDES to the AMC Ports 0 - 11 (Port 0 via GbE Switch)
    - 10 lanes of SERDES to the FMC0 Ports 0 - 9
    - 10 lanes of SERDES to the FMC1 Ports 0 - 9
    - Dual FMC HPC Connectors (downward compatible to LPC) fully pinned out to the FPGA with independent configurable power rails
    - 4 - User LEDs plus configuration DONE and INIT LEDs
    - 7 – User DIP switches for customer board configuration/ID
    - JTAG to the front via flex cable or backplane JSM
    - On-board SERDES reference clock generation
    - FPGA (soft-core CPU) RS-232 front port
    - Ordering option for LVDS usage of AMC Port 3/FCLKA instead of GTX usage
- iMX6 Quad Core CPU
    - FPGA QSPI flash mux control for field upgrade via iMX6/Ethernet
    - 1000Base-X Ethernet to AMC Port 0 (via GbE Switch)
        - 88E1512 RGMII-to-1000Base-X PHY
    - 2GB DDR3 SDRAM
    - 4MB CPU QSPI flash for boot loader (AT25DF321A-SH-T or equivalent)
    - 8GB NAND Flash for file system storage (MT29F64G08CBA or equivalent)
    - SD Card socket
    - Real-Time Clock (DS1342)
    - CPU RS-232 front port
- GbE Switch on-board which bridges the iMX6 CPU and FPGA to AMC Port 0
- AMC MMC controller w/ IPMI LEDs, hot swap handle, sensors, MGT RS-232 front port

2.1 Block Diagram

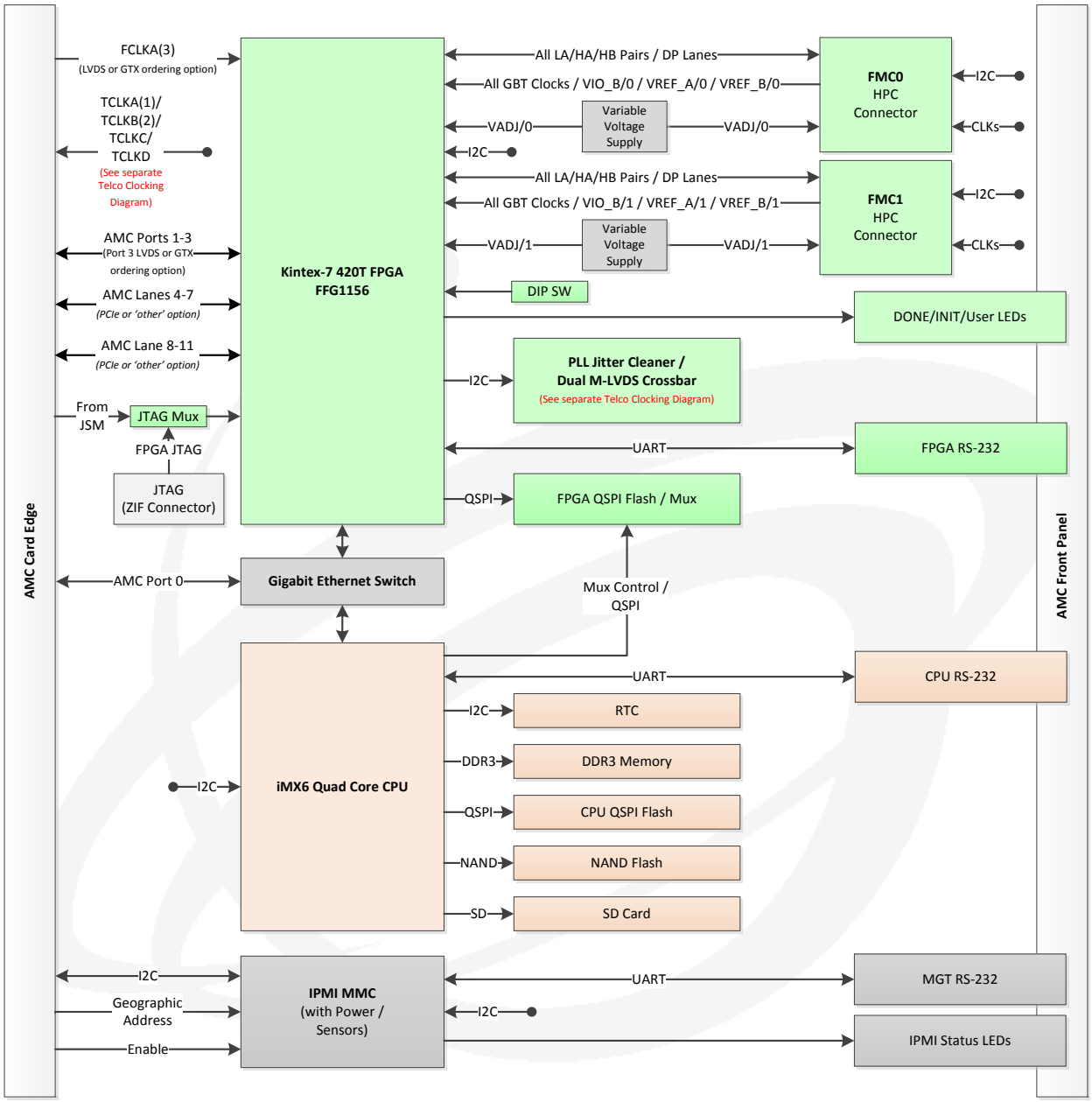

Figure 1: AMC502 block diagram

2.2 Telco Clocking Diagram

The AMC502 board includes sophisticated M-LVDS / LVDS clock routing and PLL capabilities as shown in the diagram below.

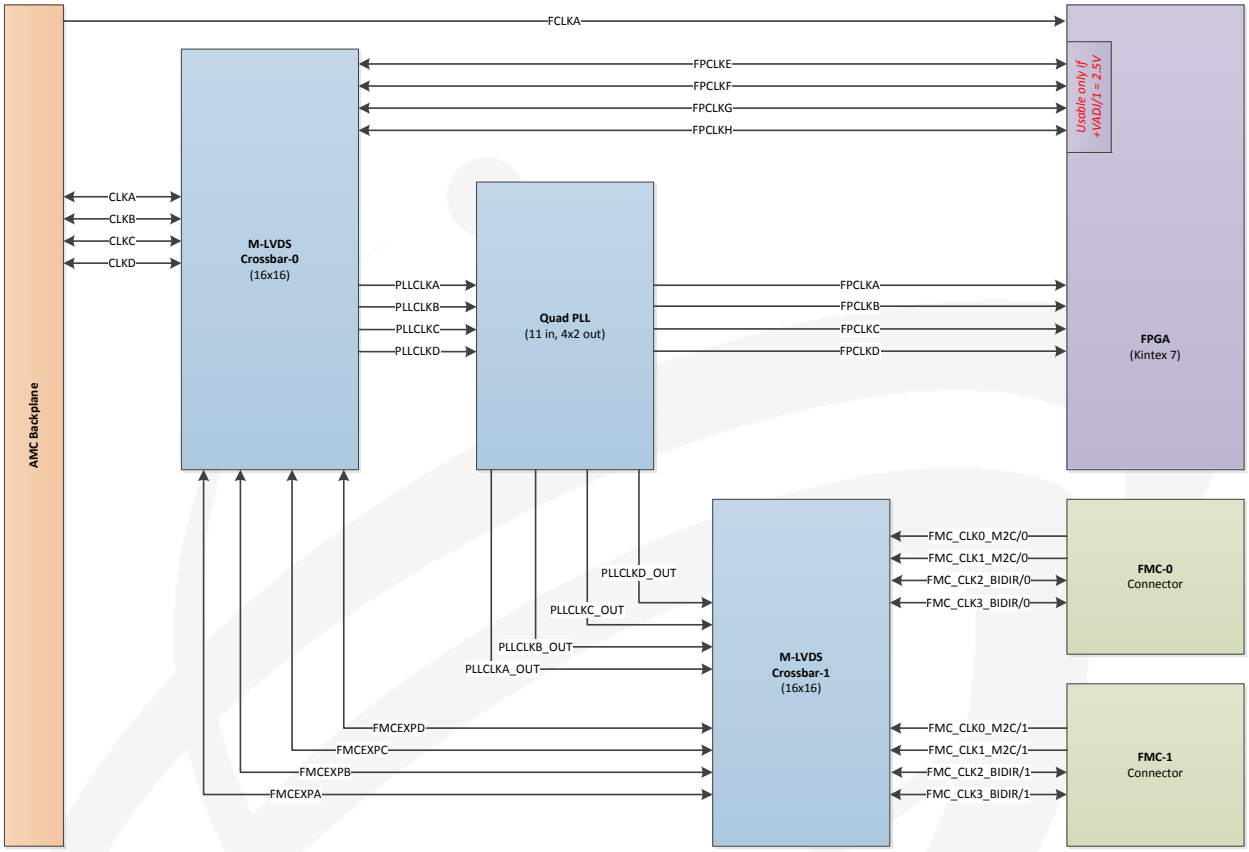

Figure 2: Telco Clocking Diagram

The M-LVDS Crossbar switches and Quad PLL are configured via I2C from the FPGA.

2.3 FPGA Banking

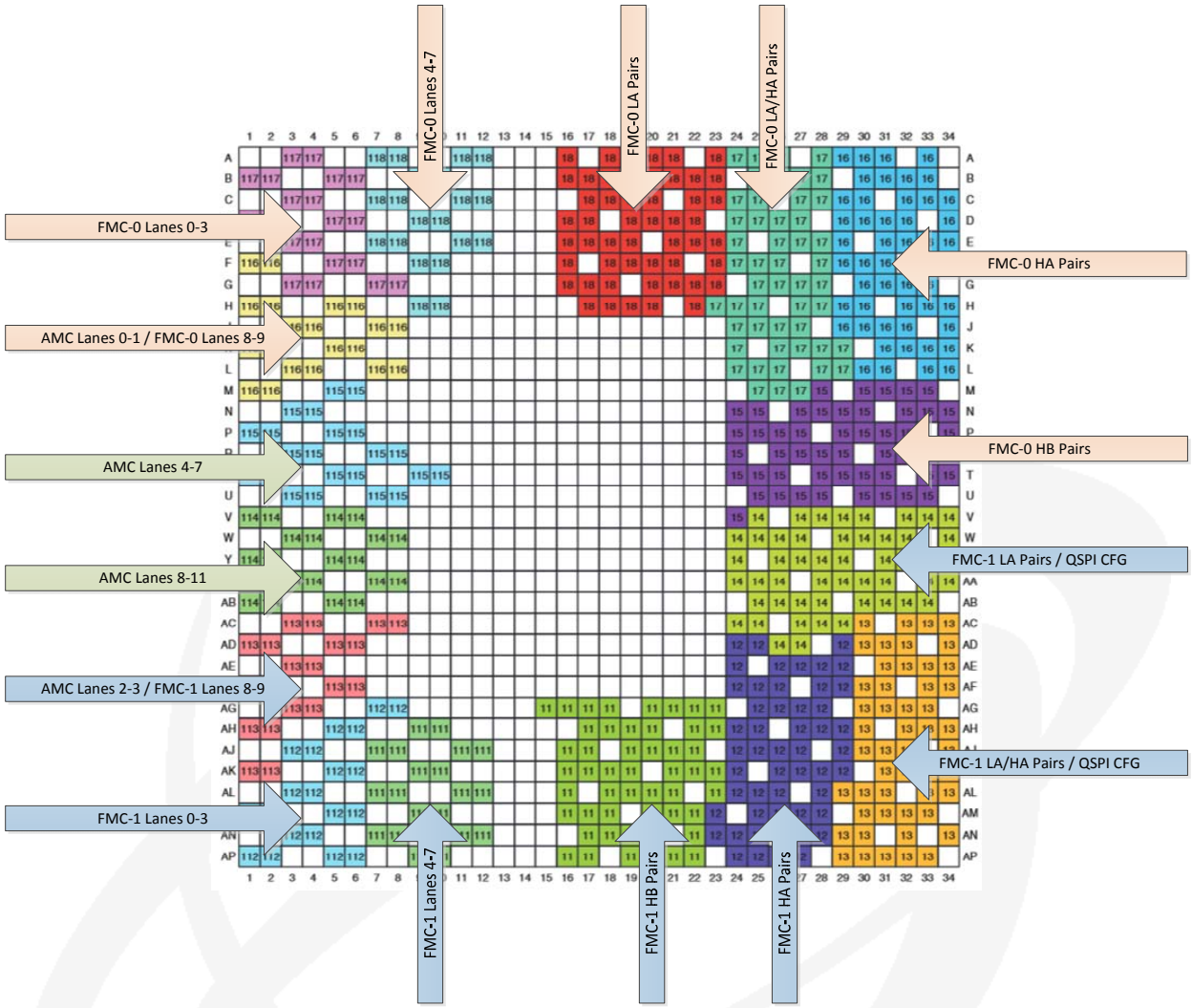

Figure 3: AMC502 Kintex-7 FPGA Banking

2.4 FPGA Floorplan

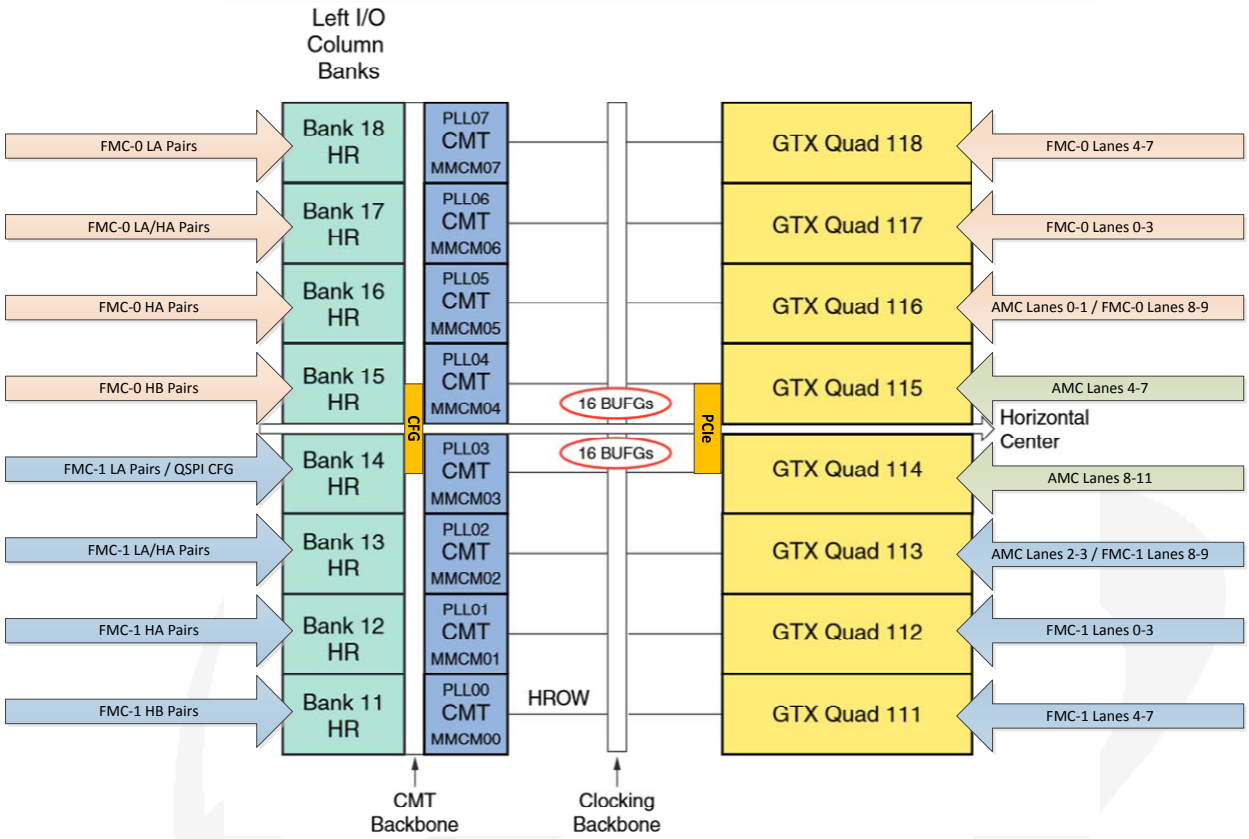

Figure 4: AMC502 Kintex-7 FPGA Floorplan

2.5 Board Layout

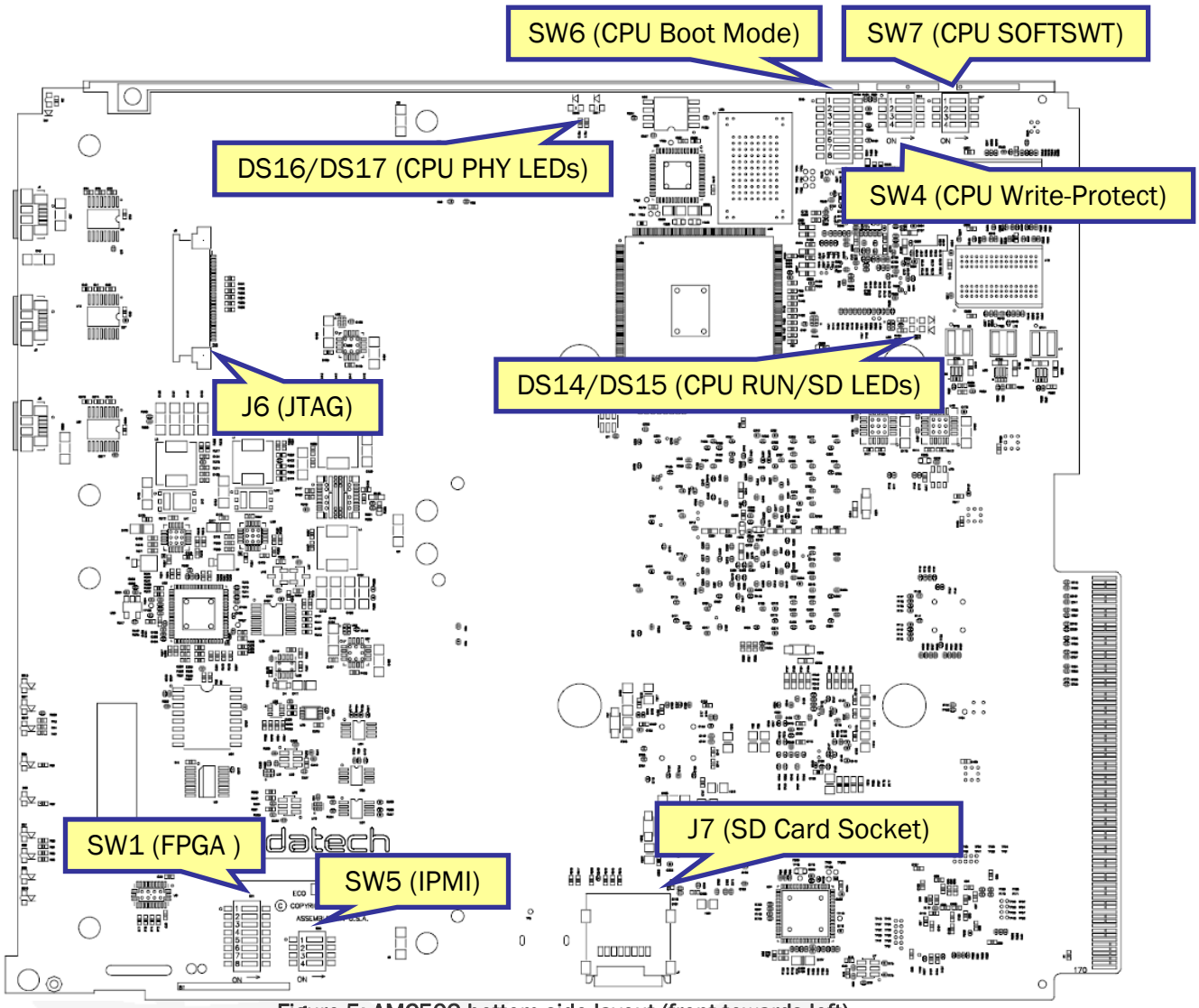

Figure 5: AMC502 bottom-side layout (front towards left)

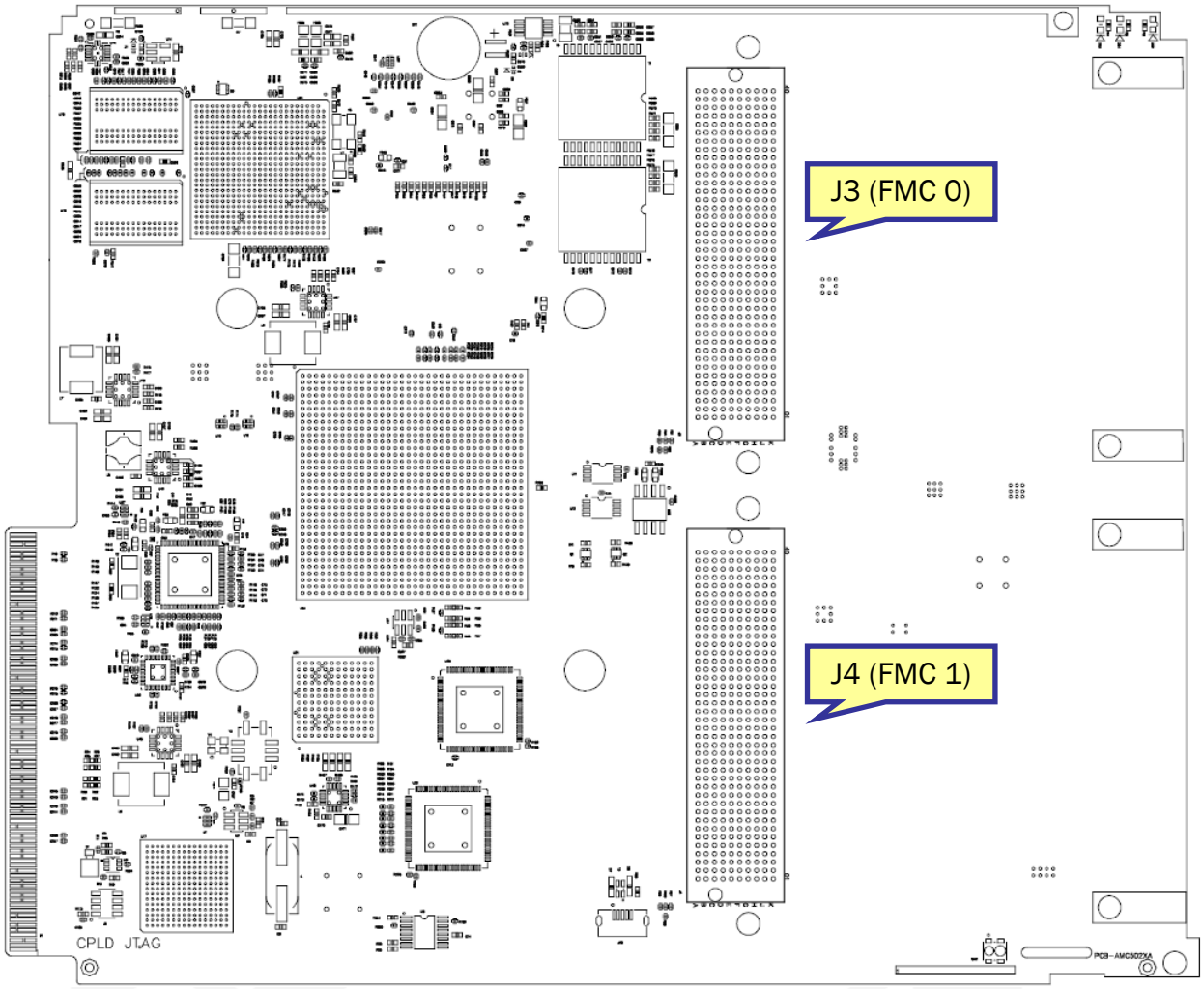

Figure 6: AMC502 top-side layout (front towards right)

The DA234 debug extender provides the headers for FPGA JTAG tools used for development/board programming.

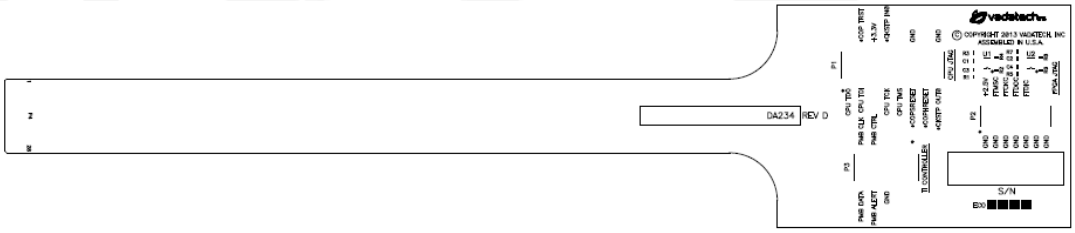

Figure 7: DA234 Rev D debug extender

2.6 Front Panel Interfaces

The front panel of the AMC502 is shown below:

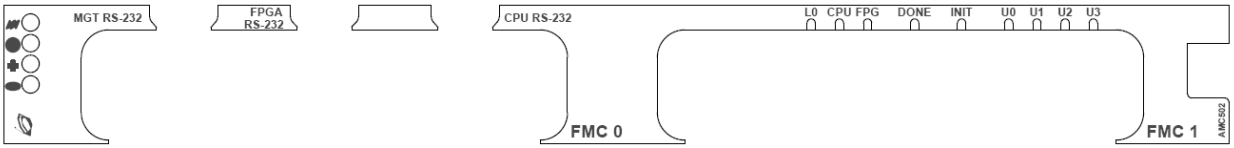

Figure 8: AMC502 front panel

2.6.1 Front Panel IPMI LEDs and Hot-Swap Handle

The front panel includes the standard AMC IPMI LEDs showing hot-swap status and general card health. The LEDs behave as follows:

LED	Off	On	Blink
Blue	Card active	OK to remove	Hot-swap/power transitioning
Red	No Fault	Payload Power Fault	n/a
Green	No payload power	Payload power OK	n/a
Amber	Normal	n/a	MMC flash writing

Table 2: AMC LED behavior

NOTE: The card should only be removed from a running carrier when the IPMI Blue LED is solid ON.

To insert the card, pull out the hot-swap handle until it stops. Insert the card into the carrier's guide rails and push on the front panel firmly until it is fully seated into the connector. If the card does not go fully in, do not force it and instead remove it and check for proper orientation or obstructions. Once fully inserted the Blue LED should go to solid ON while the Green LED should start blinking. Then push in the handle to latch the card into the carrier, the Blue LED should blink for a time and then go solid OFF while the Green LED goes solid ON.

To remove the card, pull out the hot-swap handle until it stops to unlatch the card from the carrier (but do not pull hard enough to remove the card itself yet). The Blue LED should blink for a time and then go solid ON. Once it does, pull the hot-swap handle straight out firmly to remove the card from the carrier.

2.6.2 Front Panel MGT RS-232 Port

An MGT RS-232 port is provided on the front panel for connecting to the IPMI MMC CPU. This port is used for diagnostic output of the MMC.

A VadaTech cable (P/N CBL-DB9MUSB1) is available for converting this port into a DB9 serial port. The port setup is 115200-8-N-1-NOFLOW. The pin-out is as follows:

Pin	Signal
1	n.c.
2	RXD
3	TXD
4	n.c.
5	GND
SHIELD	CGND

Table 3: MGT RS-232 port pin-out

WARNING: *This port uses the MicroUSB form factor but DOES NOT carry USB signaling. Therefore please be careful not to attach any USB device to the AMC502 board as damage could result.*

2.6.3 Front Panel Mezzanine Access

The front panel includes two cut-outs which provide front panel accessibility for the front panel of the two FMCs.

2.6.4 Front Panel CPU RS-232 Port

A CPU RS-232 port is provided as the serial console for use with the on-board iMX6 CPU.

A VadaTech cable (P/N CBL-DB9MUSB1) is available for converting this port into a DB9 serial port. The port setup is 115200-8-N-1-NOFLOW typically. The pin-out is as follows:

Pin	Signal
1	n.c.
2	RXD
3	TXD
4	n.c.
5	GND
SHIELD	CGND

Table 4: CPU RS-232 port pin-out

WARNING: *This port uses the MicroUSB form factor but DOES NOT carry USB signaling. Therefore please be careful not to attach any USB device to the AMC502 board as damage could result.*

2.6.5 Front Panel FPGA RS-232 Port

An FPGA RS-232 port is provided as the serial console for use with an FPGA soft-core CPU such as MicroBlaze.

A VadaTech cable (P/N CBL-DB9MUSB1) is available for converting this port into a DB9 serial port. The port setup is 115200-8-N-1-NOFLOW typically. The pin-out is as follows:

Pin	Signal
1	n.c.
2	RXD
3	TXD
4	n.c.
5	GND
SHIELD	CGND

Table 5: FPGA RS-232 port pin-out

WARNING: *This port uses the MicroUSB form factor but DOES NOT carry USB signaling. Therefore please be careful not to attach any USB device to the AMC502 board as damage could result.*

2.6.6 Front Panel and On-Board Payload LEDs

A green FPGA 'DONE' LED is lit to indicate that the FPGA fabric configuration loaded successfully.

A red FPGA 'INIT' LED is lit to indicate an initialization error of the FPGA or that configuration has not yet been attempted.

The front panel includes four green user-defined LEDs (U0 through U3) which are controlled via the FPGA fabric. Please refer to the VadaTech AMC502 FPGA Reference Design Manual for details on how the default reference design images use these LEDs.

The front panel also includes three GbE Switch Link/Activity LEDs:

- AMC Port 0 link/activity (L0)
- iMX6 link/activity (CPU)
- FPGA link/activity (FPG).

The following additional LEDs can be found on the bottom of the board:

- Green CPU RUN LED (DS14)
- Green SD Card LED (DS15)

The following additional LEDs can be found on the top of the board:

- Green CPU Ethernet RGMII PHY link/activity indicators (DS16/DS17)

2.7 DIP Switches

The board includes a DIP switch at SW1 with the following FPGA-related functions:

SW1-	Off	On
1	Route FPGA JTAG to J6 [factory default]	Route FPGA JTAG to Backplane JSM
2	USER0 FPGA input '1' [factory default]	USER0 FPGA input '0'
3	USER1 FPGA input '1' [factory default]	USER1 FPGA input '0'
4	USER2 FPGA input '1' [factory default]	USER2 FPGA input '0'
5	USER3 FPGA input '1' [factory default]	USER3 FPGA input '0'
6	USER4 FPGA input '1' [factory default]	USER4 FPGA input '0'
7	USER5 FPGA input '1' [factory default]	USER5 FPGA input '0'
8	USER6 FPGA input '1' [factory default]	USER6 FPGA input '0'

Table 6: SW1 settings

NOTE: When one or more FMC modules are mounted they are included in the JTAG chain. The FMCs must pass the JTAG chain through for the baseboard JTAG to work properly.

The board includes a DIP switch at SW4 with the following CPU-related functions:

SW4-	Off	On
1	Reserved [factory default]	Reserved
2	CPU NAND Flash Read/Write [factory default]	CPU NAND Flash Read-Only
3	CPU QSPI Flash Read/Write [factory default]	CPU QSPI Flash Read-Only
4	CPU SD Card Read-Only	CPU SD Card Read/Write [factory default]

Table 7: SW4 settings

The card provides a set of DIP switches at SW5 which are for IPMI-related functions and are reserved for VadaTech use.

SW5-	Off	On
1	Reserved [factory default]	Reserved
2	Reserved [factory default]	Reserved
3	Reserved [factory default]	Reserved
4	Reserved [factory default]	Reserved

Table 8: SW5 settings

Please do not change the SW5 settings unless instructed to do so by VadaTech.

The card provides a set of DIP switches at SW6 which control the iMX6 CPU boot-up.

SW6[1:8]	Meaning
ON-OFF-ON-OFF-OFF-ON-ON-OFF	Boot from QSPI [factory default]
OFF-ON-OFF-ON-ON-OFF-ON-OFF	Boot from SD Card
ON-OFF-ON-OFF-OFF-ON-OFF-ON	Boot from USB

Table 9: SW6 settings

The card provides a set of DIP switches at SW7 which are general-purpose inputs to the iMX6 CPU.

SW7-	Off	On
1	SOFTSWT0 ‘1’	SOFTSWT0 ‘0’ [factory default]
2	SOFTSWT1 ‘1’ [factory default]	SOFTSWT1 ‘0’
3	SOFTSWT2 ‘1’ [factory default]	SOFTSWT2 ‘0’
4	SOFTSWT3 ‘1’ [factory default]	SOFTSWT3 ‘0’

Table 10: SW7 settings

2.8 FMC Connectors

The AMC502 card includes two FMC HPC mezzanine connectors at J3 (FMC0) and J4 (FMC1) which are compliant with the FMC specification. These connectors provide expansion from the FPGA on the carrier board to I/O mezzanine boards. FMCs with an LPC connector are also compatible but just use a sub-set of the available signals on the carrier.

Each FMC connector provides connectivity to/from the FPGA as follows:

FMC Pin Group	Support
LA	All 34 pairs (in 2 adjacent FPGA banks)
HA	All 24 pairs (in 2 adjacent FPGA banks)
HB	All 22 pairs (in 1 FPGA bank)
DP	All 10 lanes (in 3 adjacent FPGA GTX bank)
GBTCLK0-1_M2C	Supported to GTX clocks
CLK0/1_M2C	Supported to M-LVDS Crossbar Switch
CLK2/3_BIDIR	Supported to/from M-LVDS Crossbar Switch
VREF_A_M2C	Supported (up to 2.0V)
VREF_B_M2C	Supported (up to 2.0V)
VADJ	Supported (2.5V ONLY – Contact Vadatech for others)
VIO_B_M2C	Supported (up to 3.465V)
PRSNT_M2C	Supported
PG_C2M	Supported
PG_M2C	Supported/Required
CLK_DIR	Supported
JTAG	Supported/Required
I2C FRU EEPROM	Supported (to IPMI MMC CPU only)

Table 11: FMC signals supported

Signal pins are grouped into FPGA banks based on the clock-capable signal association table found in the FMC specification in order to facilitate source-synchronous data capture schemes. LA/HA/HB signal pairs may each be used as a differential pair or as two independent single-ended signals.

For details on the actual FMC connector pin-out please refer to the related appendix later in this manual.

Please refer to the VadaTech FMCs User Manual for additional information on each VadaTech FMC.

2.8.1 FMC Mounting and Removing

Note that the FMC is NOT hot-swappable and that the AMC's face plate will need to be removed prior to mounting the FMC onto the carrier. The faceplate can be reinstalled when the FMC is mounted in its final position.

Do not attempt to force the FMC into place, but rather carefully remove the two Torx T8 screws holding the AMC faceplate to the PCB and slide the faceplate off toward the front. Then, install the FMC and reinstall the AMC's faceplate by reversing the process used to remove it. Use caution when removing the FMC from the AMC's connector. Use only upward force with no side-to-side motion to avoid damaging the connectors. Also take care to avoid damaging the AMC's IPMI LEDs which need to clear the faceplate's light-pipes as it is being removed/installed.

WARNING: *The logic design loaded into the FPGA must match the pin-out of the mounted FMCs and the power supply rails configured correctly via the MMC RS-232 interface or else damage to the carrier and/or mezzanine board may result. Such damage is NOT covered under the VadaTech warranty. Make sure of the compatibility between the FPGA image on the board, the VADJ voltage, and the FMC prior to mounting.*

2.9 On-board Debug Cable Connector

The connector at J6 is used to connect the debug cable for JTAG debugging, development, and flash programming of the FPGA using the DA234 extender board. The pin-out is as follows:

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	8	+3.3V	15	n.c.	22	n.c.
2	PMBUS_ALERT	9	n.c.	16	n.c.	23	GND
3	PMBUS_DATA	10	FTMSC	17	n.c.	24	n.c.
4	PMBUS_CLK	11	FTCKC	18	n.c.	25	n.c.
5	PMBUS_CTRL	12	FTDOC	19	n.c.	26	n.c.
6	GND	13	FTDIC	20	n.c.	27	n.c.
7	n.c.	14	GND	21	n.c.	28	GND

Table 12: J6 (Flex cable) pin-out

2.10 DA234 Debug Headers

The FPGA's JTAG header can be found on the DA234 at P2. This connector supports the Xilinx USB Platform Cable II or compatible probes. The pin-out is as follows:

Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	GND	4	FTMSC
5	GND	6	FTCKC
7	GND	8	FTDOC
9	GND	10	FTDIC
11	GND	12	n.c.
13	GND	14	n.c.

Table 13: DA234 P2 (FPGA JTAG) pin-out

The CPU JTAG header is unused for the AMC502 board.

The DA234's P3 header is for manufacturing use only.

2.11 JTAG Chain Routing

The JTAG chain routing on the board varies based on DIP switch setting and FMC module presence (based on the *PRSNT_M2C signal of the FMC connectors).

J6 Master (SW1-1 OFF), FMC0 Absent, FMC1 Absent:

J6 TDI -> FPGA TDI -> FPGA TDO -> J6 TDO

J6 Master (SW1-1 OFF), FMC0 Present, FMC1 Absent:

J6 TDI -> FPGA TDI -> FPGA TDO -> FMC0 TDI -> FMC0 TDO -> J6 TDO

J6 Master (SW1-1 OFF), FMC0 Absent, FMC1 Present:

J6 TDI -> FPGA TDI -> FPGA TDO -> FMC1 TDI -> FMC1 TDO -> J6 TDO

J6 Master (SW1-1 OFF), FMC0 Present, FMC1 Present:

J6 TDI -> FPGA TDI -> FPGA TDO -> FMC0 TDI -> FMC0 TDO -> FMC1 TDI -> FMC1 TDO -> J6 TDO

JSM Master (SW1-1 ON), FMC0 Absent, FMC1 Absent:

AMC TDI -> FPGA TDI -> FPGA TDO -> AMC TDO

JSM Master (SW1-1 ON), FMC0 Present, FMC1 Absent:

AMC TDI -> FPGA TDI -> FPGA TDO -> FMC0 TDI -> FMC0 TDO -> AMC TDO

JSM Master (SW1-1 ON), FMC0 Absent, FMC1 Present:

AMC TDI -> FPGA TDI -> FPGA TDO -> FMC1 TDI -> FMC1 TDO -> AMC TDO

JSM Master (SW1-1 ON), FMC0 Present, FMC1 Present:

AMC TDI -> FPGA TDI -> FPGA TDO -> FMC0 TDI -> FMC0 TDO -> FMC1 TDI -> FMC1 TDO -> AMC TDO

NOTE: The FMCs must at a minimum tie their TDO pin to their TDI pin if no other chips on the board require JTAG access. Otherwise the JTAG chain will be broken.

2.12 M-LVDS Crossbar Port Mapping

The M-LVDS Crossbar switch ports are mapped as follows:

Physical Port	Direction	Description
0	In or Out	Backplane CLK1 (AMC v1) / TCLKA (AMC v2)
1	In or Out	Backplane CLK2 (AMC v1) / TCLKB (AMC v2)
2	In or Out	Backplane TCLKC (AMC v2)
3	In or Out	Backplane TCLKD (AMC v2)
4	Out	PLLCLKA to Quad PLL
5	Out	PLLCLKB to Quad PLL
6	Out	PLLCLKC to Quad PLL
7	Out	PLLCLKD to Quad PLL
8	In or Out	FPCLKE to/from FPGA
9	In or Out	FPCLKF to/from FPGA
10	In or Out	FPCLKG to/from FPGA
11	In or Out	FPCLKH to/from FPGA
12	In or Out	FMCEXPA to/from M-LVDS CBS 1
13	In or Out	FMCEXPB to/from M-LVDS CBS 1
14	In or Out	FMCEXPC to/from M-LVDS CBS 1
15	In or Out	FMCEXPD to/from M-LVDS CBS 1

Table 14: M-LVDS Crossbar Switch 0 Port Mapping

Physical Port	Direction	Description
0	In or Out	FMCEXPA to/from M-LVDS CBS 0
1	In or Out	FMCEXPB to/from M-LVDS CBS 0
2	In or Out	FMCEXPC to/from M-LVDS CBS 0
3	In or Out	FMCEXPD to/from M-LVDS CBS 0
4	In	PLLCLKA_OUT from Quad PLL
5	In	PLLCLKB_OUT from Quad PLL
6	In	PLLCLKC_OUT from Quad PLL
7	In	PLLCLKD_OUT from Quad PLL
8	In	FMC0_CLK0_M2C from FMC 0
9	In	FMC0_CLK1_M2C from FMC 0
10	In or Out	FMC0_CLK2_BIDIR from FMC 0
11	In or Out	FMC0_CLK3_BIDIR from FMC 0
12	In	FMC1_CLK0_M2C from FMC 1
13	In	FMC1_CLK1_M2C from FMC 1
14	In or Out	FMC1_CLK2_BIDIR from FMC 1
15	In or Out	FMC1_CLK3_BIDIR from FMC 1

Table 15: M-LVDS Crossbar Switch 1 Port Mapping

* For “In or Out” ports please take care to set each side of the clock channel link with complimentary directionality to avoid contention.

Refer to the earlier Telco Clocking Diagram section for additional details on the clock routing.

2.13 Quad PLL Port Mapping

The reference inputs and PLL/Synthesizer outputs for the Quad PLL chip are shown below:

Physical Port	Direction	Description
REF0	In (differential)	PLLCLKA from the M-LVDS Crossbar Switch
REF1	In (differential)	PLLCLKB from the M-LVDS Crossbar Switch
REF2	In (differential)	PLLCLKC from the M-LVDS Crossbar Switch
REF3	In (differential)	PLLCLKD from the M-LVDS Crossbar Switch
REF4	In (differential)	Unused
REF5	In (differential)	Unused
REF6	In (differential)	Unused
REF7	In (differential)	Unused
REF8	In (differential)	Unused
REF9	In (single-ended)	Unused
REF10	In (single-ended)	Unused
HPDIFF0	Out	PLLCLKA_OUT to the M-LVDS Crossbar Switch
HPDIFF1	Out	FPCLKA to the FPGA
HPOUTCLK0	Out	Unused
HPOUTCLK1	Out	Unused
HPDIFF2	Out	PLLCLKB_OUT to the M-LVDS Crossbar Switch
HPDIFF3	Out	FPCLKB to the FPGA
HPOUTCLK2	Out	Unused
HPOUTCLK3	Out	Unused
HPDIFF4	Out	PLLCLKC_OUT to the M-LVDS Crossbar Switch
HPDIFF5	Out	FPCLKC to the FPGA
HPOUTCLK4	Out	Unused
HPOUTCLK5	Out	Unused
HPDIFF6	Out	PLLCLKD_OUT to the M-LVDS Crossbar Switch
HPDIFF7	Out	FPCLKD to the FPGA
HPOUTCLK6	Out	Unused
HPOUTCLK7	Out	Unused

Table 16: Quad PLL Physical Port Mapping

2.14 I2C Bus Mapping

The chips and connectors on the board are connected by various I2C buses as follows:

MMC I2C Bus Signals	CPU I2C Bus Signals	FPGA I2C Bus Signals	Slave Addr	Description	Primary Owner
SCL1 / SCL1	n.c.	SCL_L1 / SDA_L1	'XXXXX00'	FMC 0 chips following GA pin strap	MMC
			'0001100'	ZL30162 Quad PLL	FPGA
			'1011000'	IDT8V54816 M-LVDS Crossbar Switch 0	FPGA
			'1011001'	IDT8V54816 M-LVDS Crossbar Switch 1	FPGA
			Various others	Sensors/Power Controller	MMC
SCL_2 / SCL_2	I2C3_SCL / I2C3_SDA	SCL_L2 / SDA_L2	'XXXXX10'	FMC 1 chips following GA pin strap	MMC
n.c.	I2C2_SCL / I2C2_SDA	SCL_LLLX / SDA_LLLX	'1101000'	DS1342 RTC	CPU

Table 17: I2C Bus and Slave Address Mapping

NOTES:

The fixed addresses of the peripheral slave devices are shown. The MMC, CPU, and FPGA may act either as master or slave and their slave addresses are programmable (and therefore not shown here). When a bus has more than one master those masters must support multi-master arbitration.

When more than one master is on the same bus, that bus can generally be used for communication between those devices.

Some peripherals are intended to be 'owned' by certain master devices in the design and that is denoted in the chart above. Although any master on the bus may access the device, such access may interfere with the operation of the device and cause side effects on the owner of that device.

WARNING: The sensors/power controller are exclusively for use of the MMC. Do not attempt to read or write to them as this could cause unexpected behavior and they are necessary for the fundamental operation of the board. These features of the board are controlled using IPMI functionality or the MMC RS-232 port.

2.15 CPU GPIO Mapping

The following tables show the GPIO pin connections to the CPU:

GPIO1 Pin	Runtime Direction	Board Signal	Description
9	Input	SOFTSWT2	SW7-3 ON = GPIO LOW, OFF = GPIO HIGH

Table 18: CPU GPIO1 Mapping

GPIO2 Pin	Runtime Direction	Board Signal	Description
30	Output	*SS0/1	SPI Bus 1 Slave Select 0 (as GPIO)

Table 19: CPU GPIO2 Mapping

GPIO3 Pin	Runtime Direction	Board Signal	Description
20	Output	*SS0/4	SPI Bus 4 Slave Select 0 (as GPIO)
29	Output	*CPU_LED	LOW = LED ON, HIGH = LED OFF
30	Input	SOFTSWT0	SW7-1 ON = GPIO LOW, OFF = GPIO HIGH
31	Input	SOFTSWT1	SW7-2 ON = GPIO LOW, OFF = GPIO HIGH

Table 20: CPU GPIO3 Mapping

GPIO4 Pin	Runtime Direction	Board Signal	Description
31	Input	*WP/1	SW4-3 ON = GPIO LOW, OFF = GPIO HIGH

Table 21: CPU GPIO4 Mapping

GPIO5 Pin	Runtime Direction	Board Signal	Description
12	Input	*INITB+3.3V	INITB Status: Refer to Xilinx 7-Series Config Doc
13	Output	*CPU_FPGA_UPGRADE	LOW = Upgrade Mode Reset Logic, HIGH = Normal
14	Output	*CPU_FPGAPROG	PROGB Control: Refer to Xilinx 7-Series Config Doc
15	Input	DONE+3.3V	DONE Status: Refer to Xilinx 7-Series Config Doc
16	Output	*SPI_SEL_FPGA	LOW = Set Mux to attach FPGA to FPGA QSPI Flash, HIGH = Set Mux to attach CPU to FPGA QSPI Flash
17	Output	*CPU_SPI_RST	LOW = Reset FPGA QSPI Flash, HIGH = No reset
19	Input	*NAND-WPS	SW2-2 ON = GPIO LOW, OFF = GPIO HIGH

Table 22: CPU GPIO5 Mapping

GPIO7 Pin	Runtime Direction	Board Signal	Description
13	Input	SOFTSWT3	SW7-4 ON = GPIO LOW, OFF = GPIO HIGH

Table 23: CPU GPIO7 Mapping

NOTE: GPIO6 is not used for GPIO. These pins and the pins in other GPIO registers that aren't listed should be set as input and otherwise ignored. Unused pins are generally multiplexed inside of the iMX6 for use by other types of peripherals besides GPIO.

2.16 CPU UART Mapping

The VT003 supports three UART ports and corresponding modem handshake lines as shown below:

CPU UART	Purpose
UART4	CPU RS-232 Console

Table 24: CPU UART Mapping

2.17 CPU MDIO Mapping

The iMX6 CPU MDIO mapping is as follows:

MDIO address	Device
“00000”	Marvell 88E1512 RGMII-to-1000Base-T PHY

Table 25: CPU MDIO Mapping

The RGMII PHY connects to the GbE Switch on the board which bridges this port to AMC Port 0 and the FPGA via Gigabit Ethernet.

2.18 CPU SD Card Socket

An SD Card socket is provided and is attached to the iMX6 CPU’s SD1 interface.

Pin	Signal	Description
1	SD_D2	SD Card Data 2
2	SD_D3	SD Card Data 3
3	SD_CMD	SD Card Command
4	+3.3V	Power
5	SD_CLK	SD Card Clock
6	GND	Ground
7	SD_D0	SD Card Data 0
8	SD_D1	SD Card Data 1

Table 26: CPU SD Card Socket (J7) pin-out

2.19 CPU SPI Bus Mapping

The following table shows the iMX6 CPU SPI Bus mapping and externally attached SPI devices:

CPU SPI	Select Signal	Selected Device	Purpose
ECSPI1	*SS0/1	AT25DF321A 4MB QSPI Flash	CPU Boot
ECSPI4	*SS0/4	S25FL512S 64MB QSPI Flash via Mux	FPGA Configuration

Table 27: CPU SPI Bus Mapping

NOTE: The SPI chip select lines are implemented as GPIOs rather than direct SPI controller lines in order to allow them to cover multiple SPI transactions. Refer to the GPIO Mapping section for further details.

2.20 FPGA QSPI Flash Mux / Upgrade Description

The FPGA's QSPI flash sits behind a mux that allows for normal FPGA configuration/JTAG programming activities as the normal case, but that also allows the iMX6 CPU to take over the flash for purposes of upgrading it. By allowing the iMX6 to take over the flash it is possible to upgrade the FPGA's configuration via Ethernet. The mux operates as follows:

Flash Pin	*SPI_SEL_FPGA = 0 (Normal condition)	*SPI_SEL_FPGA = 1 (Upgrade from CPU override)
*CS	*FCSX signal from FPGA	*SS0/4 signal from CPU
SCK	CCLKX signal from FPGA	SCLK/4 signal from CPU
SI/IO0	D0/MOSIX signal from FPGA	MOSI/4 signal from CPU
SO/IO1	D1/MISOX signal to FPGA	MISO/4 signal from CPU
*WP/IO2	Always D02 signal from FPGA w/ external pull-up	
*HOLD/IO3	Always D03 signal from FPGA w/ external pull-up	
*RESET	Always reset signal (special behavior during upgrade mode)	

Table 28: FPGA QSPI Mux Behavior

NOTE: The FPGA has up to x4 mode access to the QSPI flash, while the CPU only has x1 mode access. Steps are taken to ensure that the FPGA's additional two I/O lines do not interfere with the CPU's operation of the flash.

As a default/normal condition the iMX6 software will leave the following pins in this state:

*CPU_FPGA_UPGRADE = HIGH (an external pull-up resistor exists on the board)
*CPU_FPGA_PROG = HIGH (an external pull-up resistor exists on the board)
*CPU_SPI_RST = HIGH (an external pull-up resistor exists on the board)
*SPI_SEL_FPGA = LOW (an external pull-down resistor exists on the board)

This condition ensures that the FPGA can configure itself from QSPI flash, the QSPI flash can be upgraded via JTAG, and the QSPI flash can be used for FPGA application storage without interference or the need to interact with the iMX6 CPU. Generally the user of the board should be able to ignore the iMX6 and use the board as a typical standalone FPGA board unless an Ethernet-based field upgrade of the flash via iMX6 CPU is underway.

2.20.1 FPGA QSPI Flash Upgrade Sequence

Only when an FPGA QSPI upgrade is initiated by the user of the iMX6 CPU will the following algorithm be followed for executing an upgrade of the FPGA QSPI flash:

1) *CPU_FPGA_PROG line is driven LOW by the CPU.

This ensures that the FPGA cannot interfere with the *WP/IO2 and *HOLD/IO3 lines of the flash chip during the upgrade and that any application running on the FPGA that may be using the flash for application storage will not be attempting to access the flash.

2) *CPU_SPI_RST line is driven LOW by the CPU.

This ensures that any persistent configuration (such as extended address bits) is reset before the CPU attempts to access the flash.

3) *CPU_FPGA_UPGRADE line is driven LOW by the CPU.

This changes the reset logic of the board such that the FPGA's assertion of *INITB does not impact the flash reset as it normally would; giving the CPU exclusive control over the flash reset assertion.

4) *SPI_SEL_FPGA line is driven HIGH by the CPU.

This connects the CPU's ECSPI4 controller to the FPGA's QSPI flash.

5) *CPU_SPI_RST line is driven HIGH by the CPU.

This takes the flash out of reset, now under control of the CPU.

6) The Linux MTD driver for the flash is loaded, flash is enumerated, and flash contents upgraded. Then the driver is removed so that it is no longer connected to the flash.

This replaces the contents of the FPGA QSPI flash with the contents provided to the upgrade application.

7) The *CPU_SPI_RST line is driven LOW by the CPU.

This ensures that any persistent configuration (such as extended address bits) is reset before the FPGA attempts to access the flash.

8) The *SPI_SEL_FPGA line is driven LOW by the CPU.

This returns control of the flash to the FPGA.

9) *CPU_FPGA_UPGRADE line is driven HIGH by the CPU.

This changes the reset logic back to normal mode where the FPGA's assertion of *INITB causes a flash reset.

10) The *CPU_SPI_RST line is driven HIGH by the CPU.

This takes the flash out of reset, now under control of the FPGA.

11) The *CPU_FPGA_PROG line is driven HIGH by the CPU.

This triggers the FPGA to configure itself from the QSPI Flash using the new image.

12) After a three second delay, the CPU checks the status of the *INITB+3.3V GPIO input to identify any possible configuration error: LOW = FAILURE, HIGH = SUCCESS. In addition to this check, the front panel FPGA RS-232 port can be used by the user to verify the version of the FPGA, etc.

3 IPMI Sensors

The AMC502 Management Controller (MMC) monitors the following sensors (refer to the software manuals for further details):

Description
AMC.0 Hot-Swap Sensor
Intake Air Temperature
Outtake Air Temperature
Board Temperature near FPGA
FPGA Die Temperature
12V Input Power
1.0V Voltage Rail
FMC Identification sensor

Table 29: MMC Sensors

In addition to these on-board sensors additional temperature sensors on specific VadaTech FMC boards are supported and may appear when sensors are listed.

4 AMC502 FMC Connector Pin-out

NOTE: The following pin-outs describe both of the FMC connectors since they share a common pin-out. When looking at the FPGA pin-out in relation to these tables, apply a /0 or /1 suffix to the signal names depending on the FMC connector being referenced.

Pin	Signal	Pin	Signal
A1	GND	B1	CLK_DIR
A2/A3	FMC/RX1+/-	B2/B3	GND
A4/A5	GND	B4/B5	FMC/RX9+/-
A6/A7	FMC/RX2+/-	B6/B7	GND
A8/A9	GND	B8/B9	FMC/RX8+/-
A10/A11	FMC/RX3+/-	B10/B11	GND
A12/A13	GND	B12/B13	FMC/RX7+/-
A14/A15	FMC/RX4+/-	B14/B15	GND
A16/A17	GND	B16/B17	FMC/RX6+/-
A18/A19	FMC/RX5+/-	B18/B19	GND
A20/A21	GND	B20/B21	FMC_GBTCLK1+/-
A22/A23	FMC/TX1+/-	B22/B23	GND
A24/A25	GND	B24/B25	FMC/TX9+/-
A26/A27	FMC/TX2+/-	B26/B27	GND
A28/A29	GND	B28/B29	FMC/TX8+/-
A30/A31	FMC/TX3+/-	B30/B31	GND
A32/A33	GND	B32/B33	FMC/TX7+/-
A34/A35	FMC/TX4+/-	B34/B35	GND
A36/A37	GND	B36/B37	FMC/TX6+/-
A38/A39	FMC/TX5+/-	B38/B39	GND
A40	GND	B40	n.c.

Table 30: J3/J4 (FMC connector) pin-out for columns A, B

NOTE: Signals shown in yellow connect to the FPGA.

Pin	Signal
C1	GND
C2/C3	FMC/TX0+/-
C4/C5	GND
C6/C7	FMC/RX0+/-
C8/C9	GND
C10/C11	FMC_LA06+/-
C12/C13	GND
C14/C15	FMC_LA10+/-
C16/C17	GND
C18/C19	FMC_LA14+/-
C20/C21	GND
C22/C23	FMC_LA18+/-CC
C24/C25	GND
C26/C27	FMC_LA27+/-
C28/C29	GND
C30	SCL (see I2C Bus Mapping)
C31	SDA (see I2C Bus Mapping)
C32/C33	GND
C34	FMC_GA0
C35/C37	+12P0V
C36	GND
C38	GND
C39	+3.3V
C40	GND

Table 31: J3/J4 (FMC connector) pin-out for column C

NOTE: Signals shown in yellow connect to the FPGA (Refer to the FPGA Pin-out). Signals shown in blue connect to other circuits on the carrier and not the FPGA. Signals shown in orange connect to the IPMI MMC/FPGA.

Pin	Signal
D1	PG_C2M
D2/D3	GND
D4/D5	FMC_GBTCLK0+/-
D6/D7	GND
D8/D9	FMC_LA01+/-CC
D10	GND
D11/12	FMC_LA05+/-
D13	GND
D14/D15	FMC_LA09+/-
D16	GND
D17/D18	FMC_LA13+/-
D19	GND
D20/D21	FMC_LA17+/-CC
D22	GND
D23/D24	FMC_LA23+/-
D25	GND
D26/D27	FMC_LA26+/-
D28	GND
D29	FMC_TCK
D30	FMC_TDI
D31	FMC_TDO
D32	AMCMP
D33	FMC_TMS
D34	*FMC_TRST
D35	FMC_GA1
D36/D38/D40	+3.3V
D37	GND
D39	GND

Table 32: J3/J4 (FMC connector) pin-out for column D

NOTE: Signals shown in yellow connect to the FPGA. Signals shown in blue connect to other circuits on the carrier and not the FPGA (but may connect indirectly).

Pin	Signal	Pin	Signal	Pin	Signal
E1	GND	G1	GND	J1	GND
E2/E3	FMC_HA01+/-CC	G2/G3	FMC_CLK1_M2C+/-	J2/J3	FMC_CLK3_BIDIR+/-
E4/E5	GND	G4/G5	GND	J4/J5	GND
E6/E7	FMC_HA05+/-	G6/G7	FMC_LA00+/-CC	J6/J7	FMC_HA03+/-
E8	GND	G8	GND	J8	GND
E9/E10	FMC_HA09+/-	G9/G10	FMC_LA03+/-	J9/J10	FMC_HA07+/-
E11	GND	G11	GND	J11	GND
E12/E13	FMC_HA13+/-	G12/G13	FMC_LA08+/-	J12/J13	FMC_HA11+/-
E14	GND	G14	GND	J14	GND
E15/E16	FMC_HA16+/-	G15/G16	FMC_LA12+/-	J15/J16	FMC_HA14+/-
E17	GND	G17	GND	J17	GND
E18/E19	FMC_HA20+/-	G18/G19	FMC_LA16+/-	J18/J19	FMC_HA18+/-
E20	GND	G20	GND	J20	GND
E21/E22	FMC_HB03+/-	G21/G22	FMC_LA20+/-	J21/J22	FMC_HA22+/-
E23	GND	G23	GND	J23	GND
E24/E25	FMC_HB05+/-	G24/G25	FMC_LA22+/-	J24/J25	FMC_HB01+/-
E26	GND	G26	GND	J26	GND
E27/E28	FMC_HB09+/-	G27/G28	FMC_LA25+/-	J27/J28	FMC_HB07+/-
E29	GND	G29	GND	J29	GND
E30/E31	FMC_HB13+/-	G30/G31	FMC_LA29+/-	J30/J31	FMC_HB11+/-
E32	GND	G32	GND	J32	GND
E33/E34	FMC_HB19+/-	G33/G34	FMC_LA31+/-	J33/J34	FMC_HB15+/-
E35	GND	G35	GND	J35	GND
E36/E37	FMC_HB21+/-	G36/G37	FMC_LA33+/-	J36/J37	FMC_HB18+/-
E38	GND	G38	GND	J38	GND
E39	+VADJ	G39	+VADJ	J39	VIO_B_M2C
E40	GND	G40	GND	J40	GND

Table 33: J3/J4 (FMC connector) pin-out for columns E, G, J

NOTE: Signals shown in yellow connect to the FPGA (refer to the FPGA pin-out). Signals shown in plum connect to the M-LVDS crossbar.

Pin	Signal	Pin	Signal
F1	PG_M2C	K1	VREF_B_M2C
F2/F3	GND	K2/K3	GND
F4/F5	FMC_HA00+/-CC	K4/K5	FMC_CLK2_BIDIR+/-
F6	GND	K6	GND
F7/F8	FMC_HA04+/-	K7/K8	FMC_HA02+/-
F9	GND	K9	GND
F10/F11	FMC_HA08+/-	K10/K11	FMC_HA06+/-
F12	GND	K12	GND
F13/F14	FMC_HA12+/-	K13/K14	FMC_HA10+/-
F15	GND	K15	GND
F16/F17	FMC_HA15+/-	K16/K17	FMC_HA17+/-CC
F18	GND	K18	GND
F19/F20	FMC_HA19+/-	K19/K20	FMC_HA21+/-
F21	GND	K21	GND
F22/F23	FMC_HB02+/-	K22/K23	FMC_HA23+/-
F24	GND	K24	GND
F25/F26	FMC_HB04+/-	K25/K26	FMC_HB00+/-CC
F27	GND	K27	GND
F28/F29	FMC_HB08+/-	K28/K29	FMC_HB06+/-CC
F30	GND	K30	GND
F31/F32	FMC_HB12+/-	K31/K32	FMC_HB10+/-
F33	GND	K33	GND
F34/F35	FMC_HB16+/-	K34/K35	FMC_HB14+/-
F36	GND	K36	GND
F37/F38	FMC_HB20+/-	K37/K38	FMC_HB17+/-CC
F39	GND	K39	GND
F40	+VADJ	K40	VIO_B_M2C

Table 34: J3/J4 (FMC connector) pin-out for columns F, K

NOTE: Signals shown in yellow connect to the FPGA (refer to the FPGA pin-out). Signals shown in plum connect to the M-LVDS CBS. Signals shown in blue connect to other circuits on the carrier and not the FPGA.

Pin	Signal
H1	VREF_A_M2C
H2	*PRSNT_M2C
H3	GND
H4/H5	FMC_CLK0_M2C+/-
H6	GND
H7/H8	FMC_LA02+/-
H9	GND
H10/H11	FMC_LA04+/-
H12	GND
H13/H14	FMC_LA07+/-
H15	GND
H16/H17	FMC_LA11+/-
H18	GND
H19/H20	FMC_LA15+/-
H21	GND
H22/H23	FMC_LA19+/-
H24	GND
H25/H26	FMC_LA21+/-
H27	GND
H28/H29	FMC_LA24+/-
H30	GND
H31/H32	FMC_LA28+/-
H33	GND
H34/H35	FMC_LA30+/-
H36	GND
H37/H38	FMC_LA32+/-
H39	GND
H40	+VADJ

Table 35: J3/J4 (FMC connector) pin-out for column H

NOTE: Signals shown in yellow connect to the FPGA (refer to the FPGA Pin-out). Signals shown in orange connect to the IPMI MMC and FPGA. Signals shown in plum connect to the M-LVDS CBS.

5 AMC502 Card-edge Pin-out

AMC Finger	Net	AMC Finger	Net	AMC Finger	Net	AMC Finger	Net	AMC Finger	Net
1	GND	35	AMC/TX3+	69	AMC/RX7-	103	AMC/TX10+	137	GND
2	AMC+12V	36	AMC/TX3-	70	GND	104	GND	138	CLKD-
3	*AMCPS1	37	GND	71	AMCSDA	105	AMC/RX11-	139	CLKD+
4	AMCMP	38	AMC/RX3+	72	AMC+12V	106	AMC/RX11+	140	GND
5	AMCGA0	39	AMC/RX3-	73	GND	107	GND	141	n.c.
6	n.c.	40	GND	74	CLKA+	108	AMC/TX11-	142	n.c.
7	GND	41	*AMCENABLE	75	CLKA-	109	AMC/TX11+	143	GND
8	n.c.	42	AMC+12V	76	GND	110	GND	144	n.c.
9	AMC+12V	43	GND	77	CLKB+	111	n.c.	145	n.c.
10	GND	44	AMC/TX4+	78	CLKB-	112	n.c.	146	GND
11	AMC/TX0+	45	AMC/TX4-	79	GND	113	GND	147	n.c.
12	AMC/TX0-	46	GND	80	FCLKA+	114	n.c.	148	n.c.
13	GND	47	AMC/RX4+	81	FCLKA-	115	n.c.	149	GND
14	AMC/RX0+	48	AMC/RX4-	82	GND	116	GND	150	n.c.
15	AMC/RX0-	49	GND	83	*AMCPS0	117	n.c.	151	n.c.
16	GND	50	AMC/TX5+	84	AMC+12V	118	n.c.	152	GND
17	AMCGA1	51	AMC/TX5-	85	GND	119	GND	153	n.c.
18	AMC+12V	52	GND	86	GND	120	n.c.	154	n.c.
19	GND	53	AMC/RX5+	87	AMC/RX8-	121	n.c.	155	GND
20	AMC/TX1+	54	AMC/RX5-	88	AMC/RX8+	122	GND	156	n.c.
21	AMC/TX1-	55	GND	89	GND	123	n.c.	157	n.c.
22	GND	56	AMCSCL	90	AMC/TX8-	124	n.c.	158	GND
23	AMC/RX1+	57	AMC+12V	91	AMC/TX8+	125	GND	159	n.c.
24	AMC/RX1-	58	GND	92	GND	126	n.c.	160	n.c.
25	GND	59	AMC/TX6+	93	AMC/RX9-	127	n.c.	161	GND
26	AMCGA2	60	AMC/TX6-	94	AMC/RX9+	128	GND	162	n.c.
27	AMC+12V	61	GND	95	GND	129	n.c.	163	n.c.
28	GND	62	AMC/RX6+	96	AMC/TX9-	130	n.c.	164	GND
29	AMC/TX2+	63	AMC/RX6-	97	AMC/TX9+	131	GND	165	AMCTCLK
30	AMC/TX2-	64	GND	98	GND	132	n.c.	166	AMCTMS
31	GND	65	AMC/TX7+	99	AMC/RX10-	133	n.c.	167	*AMCTRST
32	AMC/RX2+	66	AMC/TX7-	100	AMC/RX10+	134	GND	168	AMCTDO
33	AMC/RX2-	67	GND	101	GND	135	CLKC-	169	AMCTDI
34	GND	68	AMC/RX7+	102	AMC/TX10-	136	CLKC+	170	GND

Table 36: AMC502 card-edge pin-out

NOTE: Signals shown in yellow connect to the FPGA (refer to the FPGA Pin-out). Signals shown in blue connect to other circuits on the carrier and not the FPGA. Signals shown in plum connect to the FPGA after going through intermediate circuits (i.e. M-LVDS CBS/Quad PLL or JTAG routing). Signals shown in orange have special routing depending on ordering option A, refer to the following section for details.

6 AMC502 Ordering Option A Special Routing

Ordering option A allows for the AMC Port 3 RX/TX and AMC FCLKA/CLK3 pairs to be used as LVDS inputs instead of their normal usage. The ordering option translates as follows:

A=0 (Normal Routing):

AMC Port 3 is routed as a GTX lane to the FPGA; unavailable as LVDS RX pairs

- Backplane AMC/TX3 <= AMC/TX3 output pins of FPGA
- Backplane AMC/RX3 => AMC/RX3 input pins of FPGA

FCLKA/CLK3 is an HCSL input

- Backplane FCLKA/CLK3 (HCSL terminated) => FCLKA input pins of FPGA

FMC1 HB06 and HB21 pins available for FMC use

- FMC's FMC_HB06/1 <=> FMC_HB06/1 bi-directional pins of FPGA
- FMC's FMC_HB21/1 <=> FMC_HB21/1 bi-directional pins of FPGA

A=1 (CMS Routing):

AMC Port 3 is routed as two LVDS RX pairs; unavailable as a GTX lane

- Backplane AMC/TX3 (LVDS terminated) => AMC/TX3SEL input pins of FPGA
- Backplane AMC/RX3 (LVDS terminated) => FMC_HB21/1 input pins of FPGA

FCLKA/CLK3 is an LVDS input

- Backplane FCLKA/CLK3 (LVDS terminated) => FMC_HB06/1 and FCLKA input pins of FPGA

FMC1 HB06 and HB21 pins are unavailable for FMC use

7 AMC502 FPGA Pin-out

For details on the FPGA pin-out please refer to the pin-out spreadsheet, XDC constraint files, and top level VHDL module found in the AMC502 VHDL Sources release package. These will provide the pin locations, I/O voltages and terminations, and directionality of all of the supported FPGA pins.