ZL30162
Network Synchronization Clock Translator
Data Sheet

March 2015

Features

- Fully compliant SEC (G.813), EEC (G.8262) and Stratum 3E flexible rate conversion DPLL
- Four programmable digital PLLs/Numerically Controlled Oscillators (NCOs)
- Synchronize to any clock rate from 1 Hz to 750 MHz
- Four programmable synthesizers generate any clock rate from 1 Hz to 750 MHz with maximum jitter below 0.61ps RMS
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLLs filter jitter from 0.1 mHz up to 1 kHz
- Automatic hitless reference switching and digital holdover on reference fail
- Nine input references configurable as single ended or differential and two single ended input references
- Any input reference can be fed with sync (frame pulse) or clock

Ordering Information

ZL30162GDG2	144 Pin LBGA	Trays
	Pb Free Tin/Silver/Copper	
	-40°C to +85°C	
	Package Size: 13 x 13 mm	

- Programmable DPLLs can synchronize to sync pulse and sync pulse/clock pair
- Eight LVPECL outputs and eight LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Customer defined default device configuration available via OTP (One Time Programmable) memory, including input/output frequencies
- Dynamically configurable via SPI/I2C interface and volatile configuration registers

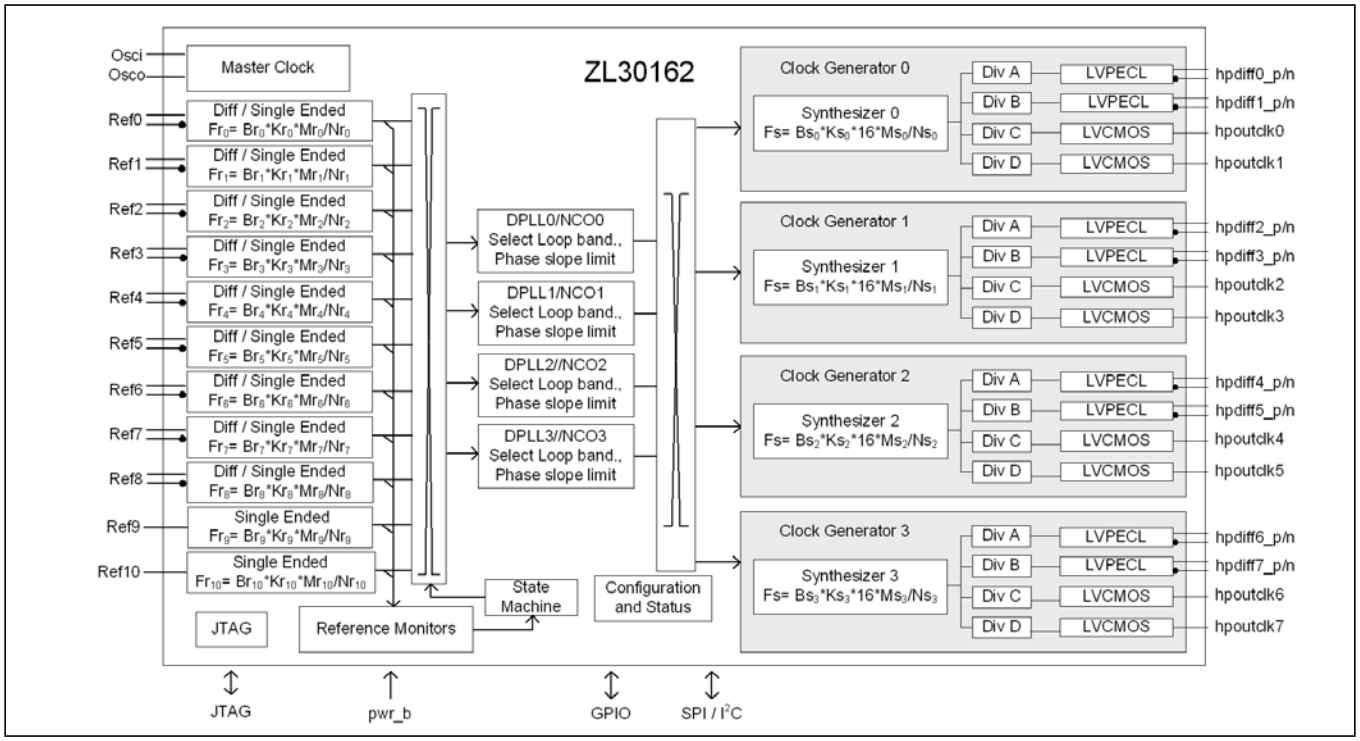


Figure 1 - Functional Block Diagram

Applications

- SyncE/SONET/SDH Timing Cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fibre Channel, XAUI

Change History

Below are the changes from the September 2014 issue to the March 2015 issue:

Page	Item	Change
1	Added Features bullet	Included availability of customer defined default configurations
12	GPIO pin descriptions	Updated GPIO [5:6] power-up settings
18	Precise Frequency Monitor (PFM)	Clarified PFM measurement interval
19	Guard Soak Timer (GST)	Corrected the GST description
33	Figure 14 "Typical Power-Up Reset and Configuration Circuit"	Updated GPIO [5:6] power-up settings
34	5.1, “ZL30162 Configuration programming“	Added section 5.1
104	Register Name: phasemem_limit_ref0	Correct the 1ms phase memory limit example in the register description
109	Register Name: page_sel_register	Added description for page 5 registers (0x280-0x2FF)
167	Register Name: dpll0_df_offset	Corrected the f_out equation in the register descritpion
227	13.0, “Package Markings“	Added section 13.0 for package markings

Below are the changes from the February 2014 issue to the September 2014 issue:

Page	Item	Change
224	Lock Time	Changed the maximum lock time for a bandwidth of 0.1 Hz and PSL of 0.885 microseconds/s from 20 seconds to 50 seconds. Changed the maximum lock time for a bandwidth of 3.6 Hz and PSL of 7.5 microseconds/s from 30 seconds to 50 seconds.
57, 104	Registers: phasemem_limit_ref0 - phasemem_limit_ref10 (0x06A to 0x074)	Corrected default value from 0x0A to 0x1B

Below are the changes from the January 2014 issue to the February 2014 issue:

Page	Item	Change
1	Features	Added Stratum 3E compliance to the feature list
23	Frequency Synthesis Engine	Added paragraph to match note 2 from register 0x1BA-0x1BB
54	Register Map	Added the Basic Procedure for Refreshing Latest Device Status from Sticky Read (StickyR) Registers when using an Interrupt Handler (event or polling)

Page	Item	Change
121	Register 0x0DC	Corrected register name
144	Register 0x12A	Corrected register name
187	Quadrature Phase Shift	Added a note to the register description of the Quadrature phase shift
217	Input to Output Timing	Removed parameter T_{REFD}
217	Input to Output Timing	Added parameter $T_{HP\_DIFF\_REFD}$
217	Input to Output Timing	Updated figure 28 and figure 29 to show ref<10:0> instead of ref<3:0>

Below are the changes from the October 2013 issue to the January 2014 issue:

Page	Item	Change
1	Document status	Moved from preliminary to released

Below are the changes from the September 2013 issue to the October 2013 issue:

Page	Item	Change
55	Summary Register: hw_rev_reg	Update default value
73	Register Name: hw_rev_reg	Update default value

Below are the changes from the April 2013 issue to the September 2013 issue:

Page	Item	Change
18	Precise Frequency Monitor (PFM)	Added note about non-integer frequencies
22	Section 4.3.3, “DPLL Rate Conversion Function and FEC Support“	Updated ZLAN reference
53	Basic Procedure for Refreshing Latest Device Status from Sticky Read (StickyR) Registers without Interrupt Handler	Updated heading title
100	Register Name: pfm_limit_ref1_0	Added note about non-integer frequencies
139	Register Name: dpll0_pbo_time_out	Updated descriptive text
142	Register Name: dpll1_mode_refsel	Corrected bit field length of DPLL1_mode
149	Register Name: dpll2_mode_refsel	Corrected bit field length of DPLL2_mode
157	Register Name: dpll3_mode_refsel	Corrected bit field length of DPLL3_mode
172	Register Name: synth0_freq_multiple	Added note
223	Section 10.1, “Output Clocks Jitter Generation“	Updated table titles

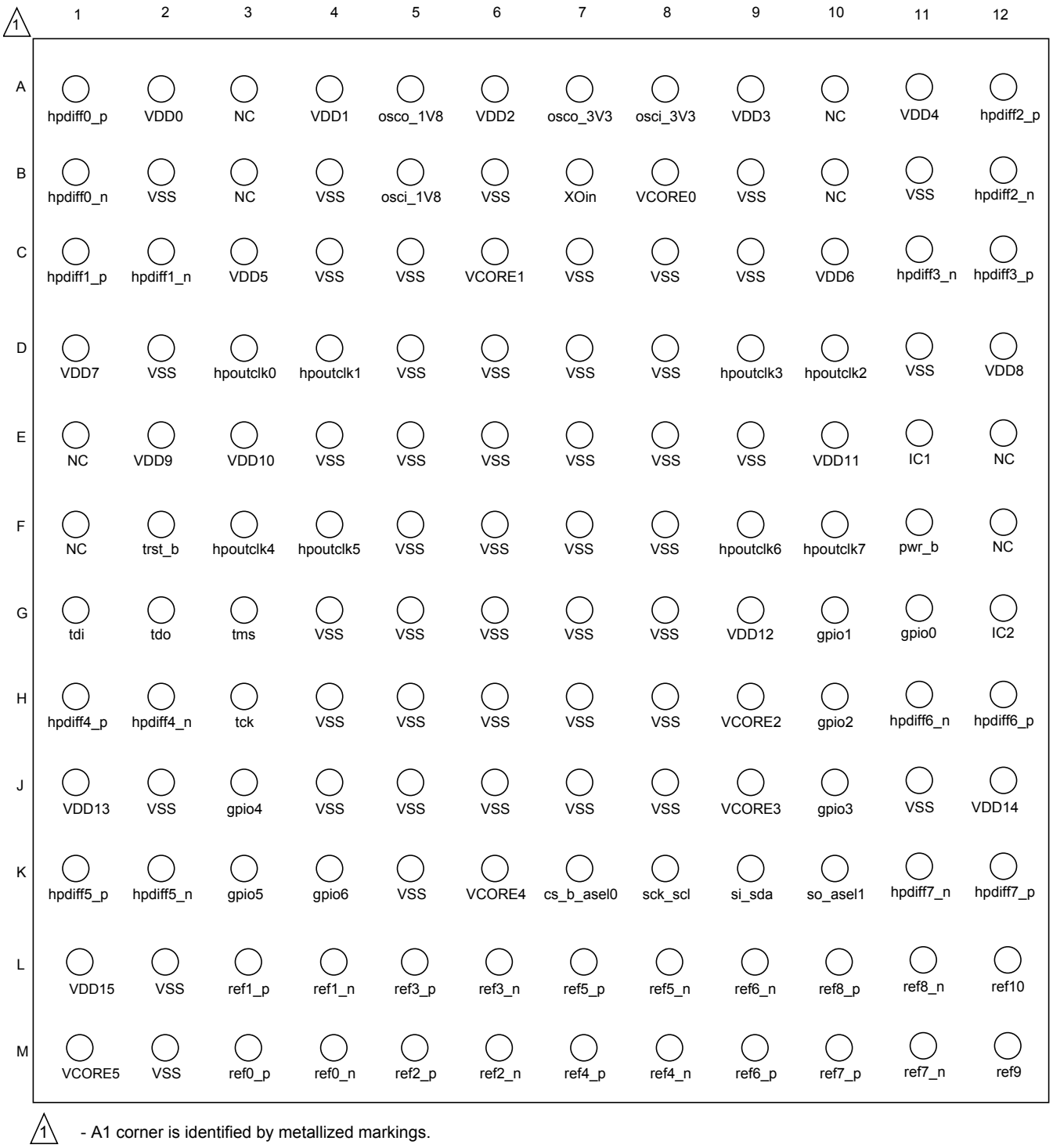
Table of Contents

List of Figures

List of Tables

1.0 Pin Diagram

TOP VIEW



1 - A1 corner is identified by metallized markings.

Figure 2 - Package Description

2.0 Pin Description

All device inputs and outputs are LVCMOS unless it is specifically stated to be differential. For the I/O column, there are digital inputs (I), digital outputs (O), analog inputs (A-I) and analog outputs (A-O).

Ball #	Name	I/O	Description
Input Reference			
M3 M4 L3 L4 M5 M6 L5 L6 M7 M8 L7 L8 M9 L9 M10 M11 L10 L11	ref0_p ref0_n ref1_p ref1_n ref2_p ref2_n ref3_p ref3_n ref4_p ref4_n ref5_p ref5_n ref6_p ref6_n ref7_p ref7_n ref8_p ref8_n	I	**Input References 0 to 8.** Input reference sources used for synchronization. The positive and negative pair of these inputs accepts a differential input signal. The refx_p input terminal accepts a CMOS input reference. These inputs can be used as an external feedback input. Maximum frequency limit on single ended inputs is 177.5 MHz, and 750 MHz on differential inputs.
M12 L12	ref9 ref10	I	**Input References 9 and 10.** Input reference sources used for synchronization. These inputs are the same as inputs 0 to 8, but only single ended. These inputs can be used as an external feedback input. Maximum frequency limit is 177.5 MHz.
Output Clocks			
D3 D4 D10 D9 F3 F4 F9 F10	hpoutclk0 hpoutclk1 hpoutclk2 hpoutclk3 hpoutclk4 hpoutclk5 hpoutclk6 hpoutclk7	O	**High Performance Output Clocks 0 to 7.** These outputs can be configured to provide any one of the single ended high performance clock outputs. Maximum frequency limit on single ended LVCMOS outputs is 177.5 MHz.

Table 1 - Pin Description

Ball #	Name	I/O	Description
A1 B1 C1 C2 A12 B12 C12 C11 H1 H2 K1 K2 H12 H11 K12 K11	hpdiff0_p hpdiff0_n hpdiff1_p hpdiff1_n hpdiff2_p hpdiff2_n hpdiff3_p hpdiff3_n hpdiff4_p hpdiff4_n hpdiff5_p hpdiff5_n hpdiff6_p hpdiff6_n hpdiff7_p hpdiff7_n	O	**High Performance Differential Output Clocks 0 to 7 (LVPECL).** These outputs can be configured to provide any one of the available high performance differential output clocks. Maximum frequency limit on differential outputs is 750 MHz.
Control and Status			
F11	pwr_b	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The **pwr_b** pin should be held low for 2 ms after all power supplies are stabilized. This pin is internally pulled-up to V_{DD}. User can access device registers either 125 ms after **pwr_b** goes high, or after bit 7 in register at address 0x000 goes high (which can be determined by polling).

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
G11 G10 H10 J10 J3 K3 K4	gpio0 gpio1 gpio2 gpio3 gpio4 gpio5 gpio6	I/O	**General Purpose Input and Output pins.** These are general purpose I/O pins. Example GPIO functions include: • DPLL lock indicators • DPLL holdover indicators • Reference fail indicators • Reference select control or monitor • Differential output clock enable • High performance LVCMOS outputs enable • Host Interrupt Output to flag status changes All GPIO functions are listed in section 5.3, “GPIO Configuration“. Pins 5:0 are internally pulled down to GND and pin 6 is internally pulled up to V_{DD}. Unused GPIO pins can be left unconnected. **After power on reset, device GPIO[0,1,3] configure basic device function. GPIO3 sets I^2C or SPI control mode, GPIO[1,0] sets master clock rate selection. The GPIO[0,1,3] pins must be either pulled low or high with an external 1 kΩ resistor for their assigned functions at reset; or they must be driven low or high for 125 ms after reset, and released and then used for normal GPIO functions.** **The GPIO4 pin must be either pulled low with an external 1 kΩ resistor; or it must be driven low for 125 ms after reset, and then released and used for normal GPIO functions.** **GPIO[5,6] are not used during power up for generic devices. For custom configured devices they select one of the four OTP configurations stored in the device and must be either pulled low or high with an external 1kohm resistor; or driven low or high for 125ms after reset, then released and used for normal GPIO functions.**
Host Interface			
K8	sck_scl	I/O	**Clock for Serial Interface.** Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I^2C mode. As an input this pin is internally pulled up to V_{DD}.
K9	si_sda	I/O	**Serial Interface Input.** The serial data input stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when host interface is configured for I^2C mode. This pin is internally pulled up to V_{DD}.
K10	so_asel1	I/O	**Serial Interface Output.** As an output, the serial stream holds the read data bits. This pin is also part of the I^2C address when the host interface is configured for I^2C mode.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
K7	cs_b_asel0	I	**Chip Select for Serial Interface.** As serial interface chip select, this is an active low signal. This pin is also part of the I^2C address select when the host interface is configured for I^2C mode.This pin is internally pulled up to V_{DD}.
JTAG (IEEE 1149.1) and Test			
G12	IC2	I	**Internal Connection**. Connect this pin to GND.
E11	IC1	A-I/O	**Internal Connection.** Leave unconnected.
G2	tdo	O	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G1	tdi	I	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
F2	trst_b	I	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be held low or pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
H3	tck	I	**Test Clock.** Provides the clock for the JTAG test logic. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
G3	tms	I	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock Note: The **osci_1V8/osco_1V8** pins are preferred to connect a crystal to the device. The **XOin** pin is preferred to connect a crystal oscillator (XO) to the device.			
A7	osco_3V3	A-O	**3.3V Crystal Master Clock Output.** For the alternative connection method for a crystal, the crystal is connected from this pin to **osci_3V3**. Not suitable for driving other devices. For clock oscillator operation or the use of a crystal between **osci_1V8** and **osco_1V8**, this pin should be left unconnected.
A8	osci_3V3	I	**3.3V Crystal Master Clock Input.** For the alternative connection method for a crystal, the crystal is connected from this pin to **osco_3V3**. For clock oscillator operation or the use of a crystal between **osci_1V8** and **osco_1V8**, this pin should be grounded.
A5	osco_1V8	A-O	**1.8V Crystal Master Clock Output.** For the primary connection method for a crystal, the crystal is connected from this pin to **osci_1V8**. Not suitable for driving other devices. For clock oscillator operation or the use of a crystal between **osci_3V3** and **osco_3V3**, this pin should be left unconnected.
B5	osci_1V8	I	**1.8V Crystal Master Clock Input.** For the primary connection method for a crystal, the crystal is connected from this pin to **osco_1V8.** For clock oscillator operation or the use of a crystal between **osci_3V3** and **osco_3V3**, this pin should be grounded.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
B7	XOin	I	**XO Master Clock Output.** For clock oscillator operation, this pin is connected to the output of the oscillator. For crystal operation using either method, this pin should be grounded.
Power and Ground			
B8 C6 H9 J9 K6 M1	V_{CORE0} V_{CORE1} V_{CORE2} V_{CORE3} V_{CORE4} V_{CORE5}		**Positive Supply Voltage.** +1.8V_{DC} nominal. These pins should not be connected together on the board. Please refer to ZLAN-327 for recommendations
A2 A4 A6 A9 A11 C3 C10 D1 D12 E2 E3 E10 G9 J1 J12 L1	V_{DD0} V_{DD1} V_{DD2} V_{DD3} V_{DD4} V_{DD5} V_{DD6} V_{DD7} V_{DD8} V_{DD9} V_{DD10} V_{DD11} V_{DD12} V_{DD13} V_{DD14} V_{DD15}		**Positive Supply Voltage.** +3.3V_{DC} nominal. These pins should not be connected together on the board. Please refer to ZLAN-327 for recommendations

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
B2 B4 B6 B9 B11 C4 C5 C7 C8 C9 D2 D11 E4 E9 G4 H4 H5 H6 H7 H8 J2 J4 J5 J6 J7 J8 J11 K5 L2 M2 D5 D6 D7 D8 E5 E6 E7 E8 F5 F6 F7 F8 G5 G6 G7 G8	V_{SS}		**Ground.** 0 Volts.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
A3 A10 B3 B10 E1 E12 F1 F12	NC		**No Connect.** These pins should be left open.

Table 1 - Pin Description (continued)

3.0 Application Example

The ZL30162 integrates features of the timing cards PLL (narrow loop bandwidth, holdover, hitless reference switching.) and Line card PLL (ultra low jitter) allowing it to be used in traditional active and redundant timing card applications or it can be used in "pizza box" application where the timing device provides both timing card and line card functionality. With four independent high performance synthesizers, the ZL30162 can provide all timing requirements for both synchronous and free run clocks. The following figure shows an example of pizza box timing source.

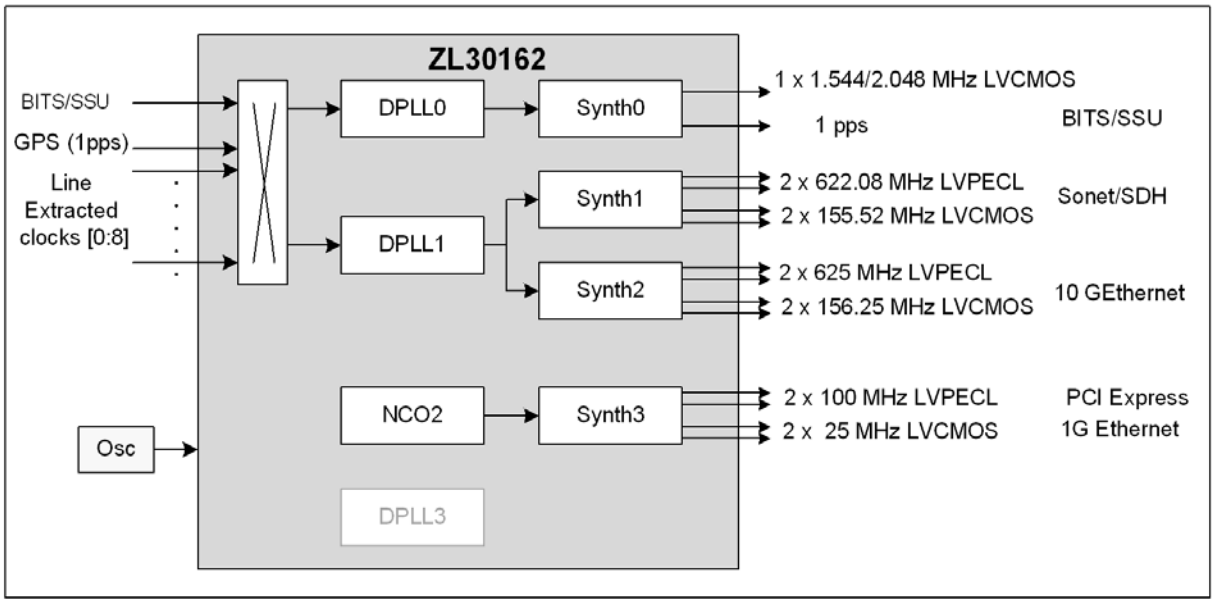


Figure 3 - Application Diagram: Total Synchronous and Free Run timing solution for telecom/datacom system

4.0 Functional Description

The functional block diagram of the device is shown in Figure 1. It's detailed operation is described in the following sections.

4.1 Input Sources

The device has twelve input sources: nine input references (single ended or differential), two single ended input references and one oscillator clock source (oscillator or crystal).

The device master clock frequency is configured on reset via external voltage levels on GPIO[1:0] pins. The recommended frequency of the master clock is 49.152 MHz.

The device synchronizes (locks) to any input reference which is a 1 Hz (1 pps), 1 kHz multiple, or it synchronizes (locks) to any input reference which is an M/N x 1 kHz multiple (FEC rate) where M and N are 16 bits wide.

The device input reference frequency is programmed during initialization, which can be changed during operation by setting the DPLL into the holdover mode before a frequency change.

The device accepts an input reference with a maximum frequency of 177.5 MHz through single ended LVCMOS input or 750 MHz frequency through differential inputs.

If the frequency of an input reference exceeds 400 MHz, the reference must be divided by 2 before being fed to DPLL (Refer to **ref_pre_divide** registers).

4.2 Input Reference Monitoring

The input references are monitored by reference monitor indicators which are independent for each reference. They indicate abnormal behavior of the reference signal, for example; drift from its nominal frequency or excessive jitter.

Loss of Signal Monitor (LOS)

LOS is an external signal, fed to one of ZL30162 GPIO pins. LOS is typically generated by a PHY device whose recovered clock is fed to one of the reference inputs. The PHY device will generate a LOS signal when it cannot reliably extract the clock from the line. The user can set one of GPIO pins as a LOS input by programming corresponding GPIO register.

Coarse Frequency Monitor (CFM)

The CFM monitors the input reference frequency for 1.25 ms so that it can quickly detect large changes in frequency. CFM limit for each input reference can be selected in corresponding **scm_cfm_limit_ref** registers with range from 0.1% to 50%. If the CFM limit is exceeded, then CFM failure is declared for corresponding reference.

For frequencies below 16 kHz, the CFM and SCM limits should be set to the same value for proper operation.

Precise Frequency Monitor (PFM)

he PFM block measures the frequency accuracy of the reference over a 10 second interval, the indicator bit is updated every second. . The PFM provides a level of hysteresis to prevent a failure indication from toggling between valid and invalid for input references that are on the edge of the acceptance range. PFM limit for each reference can be selected in the **pfm_limit_ref** registers. When determining the frequency accuracy of the reference input, the PFM uses the external master clock oscillator's frequency as its reference.

PFM supports any reference (input) frequency from 1 Hz to 750 MHz except for non integer (in Hz) frequencies below 5,000,000 Hz. For example 1 Hz, 8 kHz, 2.048 MHz, 156.25*66/64 MHz are supported frequencies but 0.5 Hz and 1.5 Hz are not supported.

The PFM limit should be set based on the following table in **pfm_limit_ref** registers:

Value	Acceptance Range	Rejection Range	Typical Application
000	+/- 9.2 ppm	+/- 12 ppm	Stratum 3, G.813 option 1, G.8262 EEC 1 & 2
100	+/- 13.8 ppm	+/- 18 ppm	
101	+/- 24.6 ppm	+/- 32 ppm	
110	+/- 36.6 ppm	+/- 47.5 ppm	
001	+/- 40 ppm	+/- 52 ppm	SONET Minimum Clock, G.813 option 2
111	+/- 52 ppm	+/- 67.5 ppm	
010	+/- 64 ppm	+/- 83 ppm	Stratum 4, G.824
011	+/- 100 ppm	+/- 130 ppm	G.823

Table 2 - Frequency Out of Range Limits

Single Cycle Monitor (SCM)

This detector measures the rising to rising edge and falling to falling edge periods of the input reference. If either exceeds the predefined SCM limit then a SCM failure is declared. The SCM limit for each input reference can be selected in the corresponding **scm_cfm_limit_ref** registers with range from 0.1% to 50%. The limits are input frequency dependent. Please refer to the description in **scm_cfm_limit_ref** registers.

For frequencies below 16 kHz, the CFM and SCM limits should be set to the same value for proper operation.

For frequencies above 400 MHz, SCM (and the GST) should not be used.

Guard Soak Timer (GST)

When selected, the guard soak timer adds extra time to qualify and disqualify a reference. The default time to wait to disqualify a reference is 50 ms after a CFM and SCM failure is detected. When qualifying a reference, the time starts when the CFM or SCM failure is cleared. The default qualification time is 4 times the disqualification time.

A PFM failure does not effect this timer.

For frequencies above 400 MHz, the GST should not be used because the single cycle monitor (SCM) will never be valid.

Holdover and Reference Switching Masks

These bit fields control which of the reference monitoring signals on the selected reference are used to trigger a reference switch or transition to holdover. The **dplln_ref_fail_mask** and **dplln_pfm_fail_mask** fields control the action taken when any of the reference monitoring signals is triggered. Please note that the GST mask bit should not be enabled without either the SCM or the CFM bit for either reference switching or holdover. Also, the holdover mask has higher priority than the reference switching mask when both have the same signal unmasked.

For return from holdover, the mask refers to the highest priority reference and will prevent the start of transition to lock mode if the indicated conditions are active.

4.3 Digital Phase Locked Loop (DPLL)

The device supports four independent digital PLL modules. All four DPLLs are enabled by default. Each DPLL can be enabled/disabled through the host registers.

With four DPLLs, the device can synchronize to four independent reference clocks.

4.3.1 DPLL General Characteristics

Pull-in Hold-in range

The DPLL supports pull-in/hold-in of +/-12 ppm, +/-52 ppm, +/-83 ppm, +/-130 ppm, +/-400 ppm or unlimited.

DPLL bandwidth (jitter/wander transfer)

The DPLL loop bandwidth is programmable from 0.1 mHz to 1 kHz with logarithmic resolution. Common cut-off frequencies are supported such as: 0.1 mHz, 1 mHz, 10 mHz, 0.1 Hz, 1.7 Hz, 5 Hz, 7 Hz, 14 Hz and many others up to 1 kHz. The DPLL bandwidth is typically determined during the initialization. When changing the bandwidth dynamically, it is recommended to put the DPLL to Holdover mode first and then change the bandwidth. After the bandwidth has been changed, the DPLL should be set to the Normal mode.

Loop bandwidth is set by programming the **dpllX_ctrl** register for seven wide loop bandwidths: 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz and 896 Hz. For low loop bandwidths, the user selects the variable loop bandwidth option in the **dpllX_ctrl** register and then programs the **dpllX_var_bw_sel** register based on targeted timing specification. Some common settings are:

Value	BW (Hz)	Application
0x60	0.1	GR-253 SONET Stratum 3, SMC, G.813 option 2, G.8262 EEC 2
0x88	1.8	GR-1244 Stratum 3, G.813 option 1
0x92	3.6	G.813 option 1, G.8262 EEC 1
0x20	1 mHz	Stratum 3E
0x0F	0.3 mHz	Wireless Basestations

Table 3 - Common Low DPLL Loop Bandwidth

For the line card bandwidths in the ZL30162 (5.2 Hz and above), it is recommended that the fast lock mode be enabled when phase slope limiting is used. It should be disabled with an unlimited PSL. This can be done in the **dplln_fast_lock_ctrl** register.

For the timing card bandwidths in the ZL30162 (below 5.2 Hz), it is recommended that the fast lock mode be enabled. This can be done in the **dplln_fast_lock_ctrl** register.

The DPLL locks to an input reference and provides a stable low jitter output clock when the selected loop bandwidth is less than 1/30th the input reference frequency. As an example, a 19.44 MHz reference could use a bandwidth up to 896 Hz, and a 1 kHz input reference could be used a loop bandwidth of up to 14 Hz. For 8 kHz reference the recommended maximum loop bandwidth is 56 Hz.

For low frequency input reference such as 1 Hz, the loop bandwidth should be set to 30 mHz or lower. It should be noted that narrower loop bandwidths require master oscillator with higher stability.

For a faster settling time when using a 1 Hz input with a final bandwidth of 1 mHz or 30 mHz , the bandwidth should be initially set to 100 mHz and the **dplln_damping_ctrl** set to 0x2. After 10 minutes, the final bandwidth and **dplln_damping_ctrl** of 0x5 should be applied.

Jitter/Wander Generation

Jitter and wander generation performances are provided in section 10.0, “Performance Characterization“.

Phase Transients and Phase Slope Limiting

When a reference switch occurs with phase tracking active (i.e., TIE clear disabled or hitless reference switching), the DPLL transitions the phase of the output smoothly, limited by the selected loop bandwidth and by the selected phase slope limit.

The device offers the following selectable phase slope limiting options: 61 usec/sec, 7.5 usec/sec, 0.885 usec/sec or unlimited. If the required phase slope limit is 0.885 usec/sec or 7.5 usec/sec, the user should first set the device to unlimited phase slope and wait for PLL to achieve lock before changing it to desired phase slope limit. The phase slope limit is set in register **dpllX_ctrl** as shown in Table 4.

dpll_phase_slope_limit	Phase Slope Limiting	Application
00	61 μs/s	GR-1244 Stratum 3
01	7.5 μs/s	G.813 option 1
10	885 ns/s	GR-1244 Stratum 2, 3E, 3 (objective)
11	Unlimited	

Table 4 - DPLL Phase Slope Limiting

Holdover Stability

DPLL initial holdover accuracy is better than 1 ppb when using 0.1 Hz or narrower loop filter.

Input Tolerance Criteria

Input tolerance indicates that the device tolerates certain jitter, wander and phase transients at its input reference while maintaining outputs within an expected performance and without experiencing any alarms, reference switching or holdover conditions. Input tolerance is associated with input reference source characteristics and the standards associated with input reference type.

DPLL Monitoring

The DPLL provides lock and holdover indicators using the default lock indicator conditions.

The lock time is dependent on employed loop bandwidth. The device has a lock time of less than 2 sec for loop bandwidths larger or equal than 5.2 Hz and the phase slope limit set to unlimited. For the other loop bandwidths and phase slope limits please refer to Section 10.2.

4.3.2 DPLL Modes

The DPLL in the device support five modes: free-run, forced holdover, automatic, forced reference lock and numerically controlled oscillator (NCO). To lock the DPLL to a reference, automatic or forced reference mode should be used. In each of the locked modes, there are three states: acquiring, normal (locked) and holdover. (The acquiring state is temporary between the availability of a reference and the completion of the locking process.) In the automatic mode, the DPLL may go between the states depending on the availability of all the references (with a priority above "never lock"). In forced reference mode, the device will go into holdover if the reference selected is unavailable even if other references are available. The availability of a reference is determined by the reference qualification process. In the holdover state, the device provides output clocks which are not locked to an external reference signal, but are based on an estimate of the frequency during the previous time in the locked state. To force the DPLL into the holdover state even with good references present, the forced holdover mode is used.

In addition, the DPLL can be put into the free-run mode. This is used when the synchronization to a reference is not required or is not possible. Typically, this is used immediately following system power-up. In the free-run mode, the device provides timing and synchronization signals which are based on the master clock frequency only, and are

not synchronized to the reference input signals. The free-run accuracy of the output clock is equal to the accuracy of the master clock. So if a ±20 ppm free-run output clock is required, the master clock must also be ±20 ppm.

The freerun mode:

- The DPLL has to generate all its output clocks based only on the device master clock input.
- The DPLL will not lock or switch to a reference or go into holdover.
- The reference switch mask and the reference holdover mask are ignored.

The forced holdover mode:

- All references are ignored and the DPLL has to go to holdover (based on last selected reference)
- The reference switch mask and the reference holdover mask are ignored.

The forced reference lock mode:

- The DPLL will try to lock to the host-specified reference.
- The reference switch mask is ignored. No reference switching will be performed.
- If the holdover mask is set, then the device will switch to holdover if the selected reference fails.
- If the holdover mask is not set, then the device will attempt to lock to the selected reference, even if it is failing one of the reference monitors.

The automatic mode:

- Reference selection and holdover is automatically handled by the device, based on the holdover and reference switch masks, and the reference priority.
- If the reference switch mask is set, then reference will be selected based on availability and priority. If all enabled references are bad, then the device will enter holdover.
- If holdover mask is set (and ref. switch mask cleared), then device switches to holdover on ref failure.
- If neither ref switch nor holdover mask are set, then device will keep trying to lock to a failed ref.

The NCO mode:

- The DPLL is run in free-run mode. The output clock is the requested synthesizer frequency with an offset specified by the **dpll_df_offset** register. This write-only register will change the output frequency of the DPLL.

4.3.3 DPLL Rate Conversion Function and FEC Support

The DPLL provides up scaling and down scaling functions. It has the ability to switch from normal rate (before FEC is negotiated) to FEC rate and vice versa.

The DPLL supports:

- **Simple rate conversion** (i.e., take in 19.44 MHz and create 255/238 FEC SONET/SDH clock of 666.51 MHz),
- **Double rate conversion** (i.e., take in 19.44 MHz, create FEC 10 GbE clock of 644.5313, which is 66/64 rate converted 625 MHz, or create 690.5692 which is 255/238 x 66/64 rate converted 625 MHz)

The following is just an example of the frequencies that can be supported at the input and output independently (many more frequencies can be supported):

- **GbE:**
  - 25 MHz
  - 125 MHz
- **XAUI (chip to chip interface, which is a common chassis to chassis interface)**:

- 156.25 MHz or x2 or x4 version

- **OC-192/STM-64:**
  - 155.52 MHz or x2 or x4 version
  - 155.52 MHz x 255/237 (standard EFEC for long reach) or x2 or x4 version
  - 155.52 MHz x 255/238 (standard GFEC for long reach) or x2 or x4 version
- **10 GbE:**
  - 156.25 MHz which is 125 MHz x 10/8 or x2 or x4 version
  - 155.52 MHz x 66/64 or x2 or x4 version
  - Long reach 10 GE might require the following frequencies with simple rate conversion: (156.25 MHz x 255/237) and (156.25 MHz x 255/238).
  - The following frequencies with double rate conversion: (155.52 MHz x 66/64 x 255/237) or (155.52 MHz x 66/64 x 255/238) and (156.25 MHz x 66/64 x 255/238) or (156.25 MHz x 66/64 x 255/238). Also, user can use x2 or x4 version of the listed frequencies.

Application Note ZLAN-447 explains how to generate the most common frequencies.

4.3.4 DPLL Input to Output and Output to Output Phase Alignment

Techniques offered for Phase Alignment

When the output clock is locked to a jitter free and wander free input clock, input to output latency is expected to have a typical error of 0 nsec.

The coarse and fine phase adjustments allow for input to output and output to output latency corrections to compensate for PCB load delay, as detailed in 4.5, “Dividers and Skew Management“.

The PLL architecture allows for implementation of an external feedback (external output clock phase sense) of the PLL path that is fed through one of the available references. Such external feedback would allow for dynamic changes of PCB routing and external buffer delay caused by changes in temperature.

It is recommended that the DPLLs be fully configured before enabling external feedback. If a synthesizer or DPLL in the external feedback path need to be reconfigured, disable external feedback before changing the parameters and then enable external feedback.

4.4 Frequency Synthesis Engine

The device frequency synthesizers can generate output clocks which meet the jitter generation requirements for various timing requirements detailed in section 10.0, “Performance Characterization“.

The frequency synthesis engines can generate any clock frequency between 1 GHz and 1.5 GHz. The frequency for each synthesizer is programmed as 16 * B * K * M/N Hz where B, K, M and N are 16 bits wide registers.

For proper operation of the synthesizer, Bs x Ks x Ms / Ns must not be an integer multiple of 65,536,000;

69,632,000; 73,728,000; 77,824,000; 81,920,000; 86,016,000 or 90,112,000.

4.5 Dividers and Skew Management

Each frequency synthesizer has four independent output dividers. Two dividers are associated with differential LVPECL outputs that can generate clocks from 1 Hz to 750 MHz and the other two dividers are associated with single ended LVCMOS outputs that can generate clocks between 1 Hz and 177.5 MHz.

Each synthesizer with associated dividers supports fine and coarse phase (skew) adjustment of output clocks. The fine phase adjustment affects equally all four outputs driven by a particular synthesizer, while the coarse phase affects independently each LVCMOS output.

The fine phase adjustment allows the user to advance simultaneously all four outputs of each synthesizer in 256 steps where each step is 1/256 of the Synthesizer clock period. For example if the synthesizer is programmed to generate 1.5GHz clock, the maximum fine advancement is 666.6 ps with the step size of only 2.6 ps.

The coarse phase adjustment allows the user to advance or delay each LVCMOS output in steps equal to the period of the synthesizer clock frequency with the maximum range equal to +/-4096 synthesizers clock periods. For example, if the synthesizer is programmed to generate 1.5 GHz clock, the step size will be 1/1.5GHz = 666.6ps and the maximum range will be +/-4096 * 666.6 ps.

4.6 Output Clocks Configuration

Figure 4 shows relationship between synthesizers, dividers and output dividers.

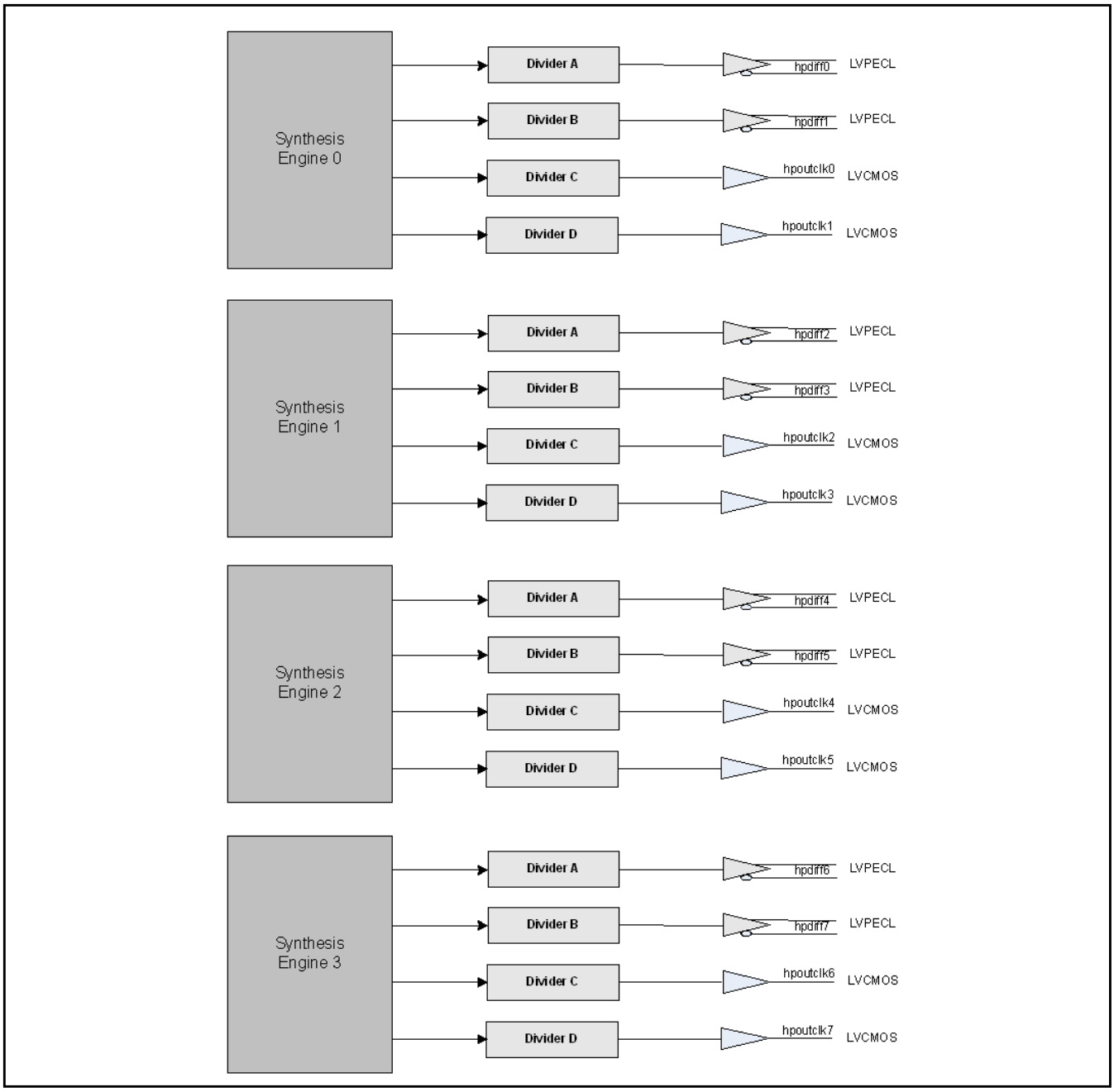


Figure 4 - Output Clocks Configuration

4.7 Output Drivers

The device has eight high performance differential (LVPECL) outputs. and eight high performance single ended outputs.

The high performance single ended driver (LVCMOS) supports a maximum clock frequency of 177.5 MHz and the high performance differential driver (LVPECL) supports a maximum clock frequency of 750 MHz, the jitter performance is detailed in section 10.0, “Performance Characterization“.

The LVPECL outputs should be terminated as shown in Figure 5. Terminating resistors provide 50 Ω equivalent Thevenin termination as well as biasing for the output LVPECL driver. Terminating resistors should be placed as close as possible to input pins of the LVPECL receiver. If the LVPECL receiver has internal biasing then AC coupling capacitors should be added.

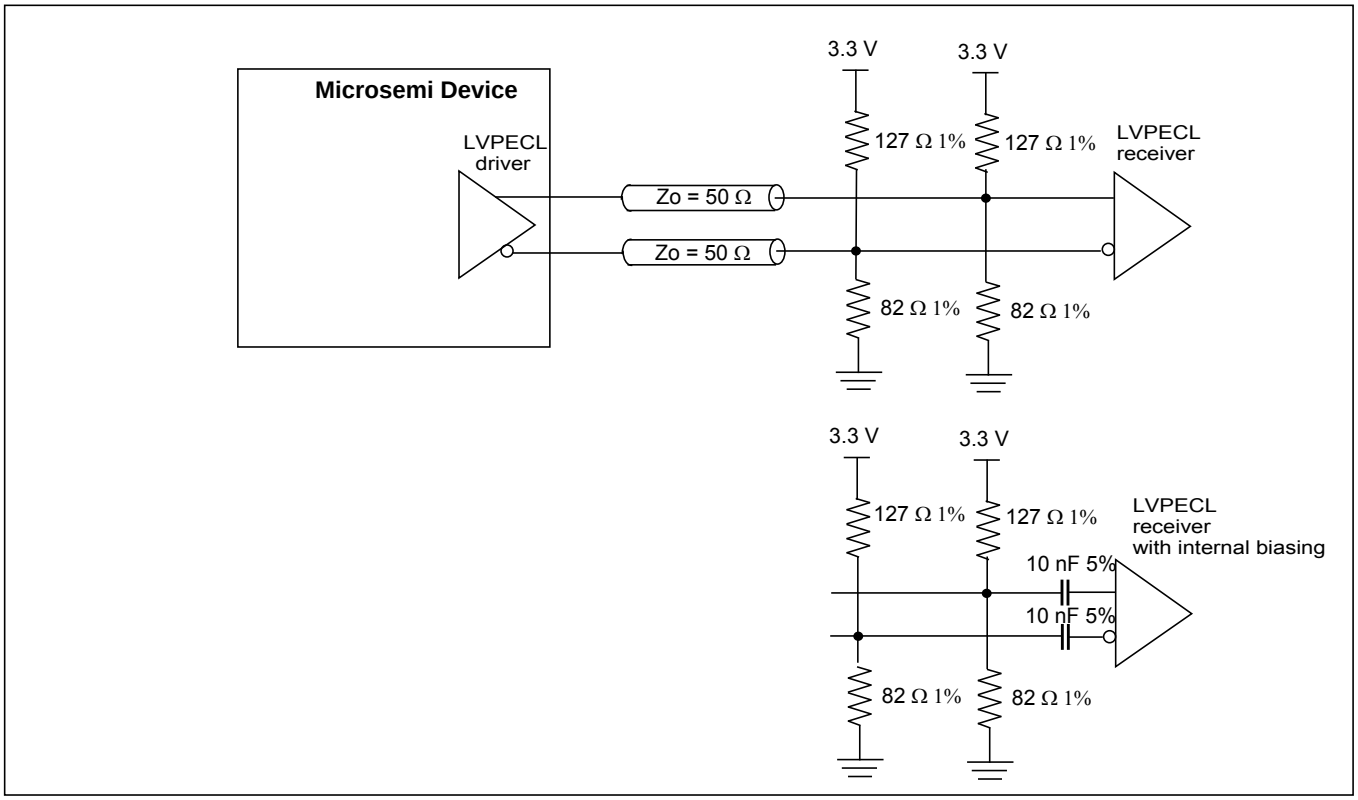


Figure 5 - Terminating LVPECL Outputs

If the transmission line is required to be AC coupled then the termination shown in Figure 6 should be implemented. 200 Ω resistors are used to provide DC biasing for LVPECL driver. Both AC coupling capacitor and biasing resistors should be placed as close as possible to output pins.

Thevenin termination (127 Ω and 82 Ω resistor) provide 50 Ω termination as well as biasing of the input LVPECL receiver. If the LVPECL receiver has internal DC biasing then the line should be terminated with 100 Ω termination resistor between positive and negative input. In both cases termination resistors should be places as close as possible to the LVPECL receiver pins. Some LVPECL receivers have internal biasing and termination. In this case no external termination should be present.

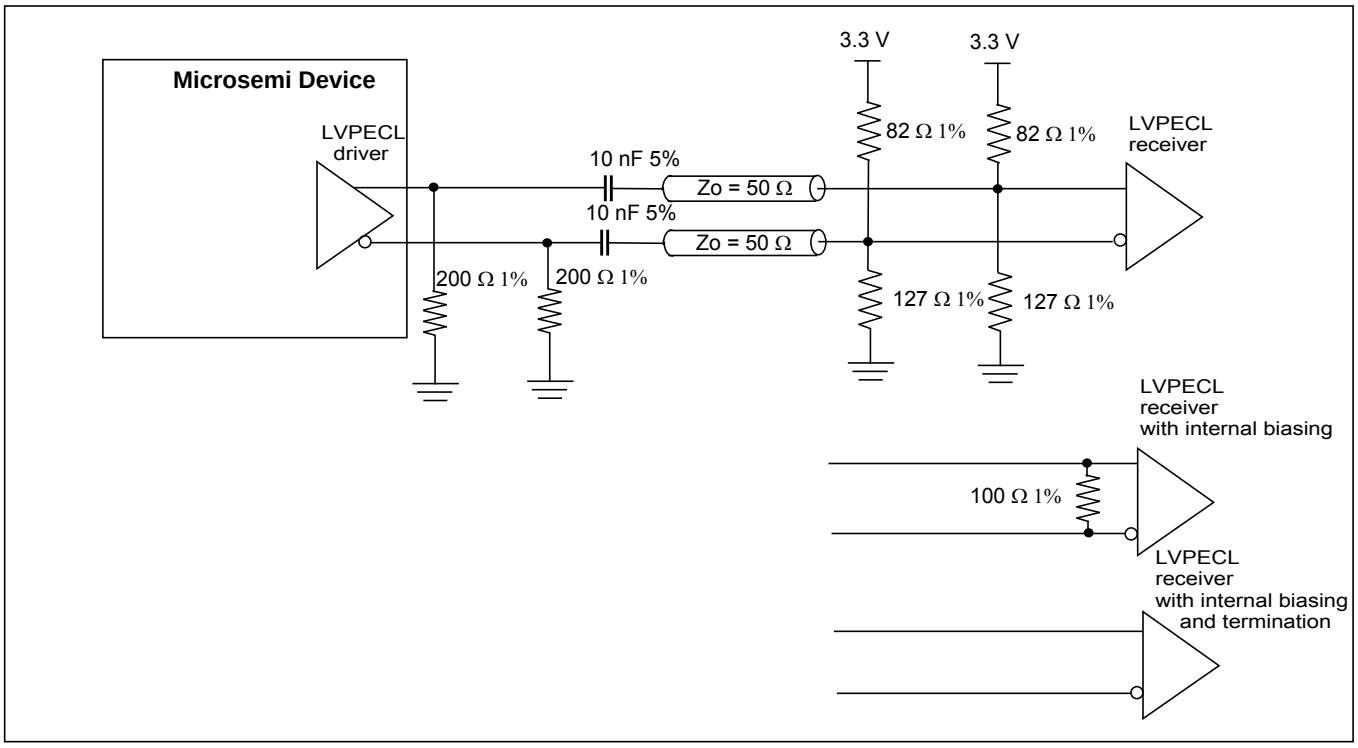


Figure 6 - Terminating AC coupled LVPECL outputs

High performance LVCMOS outputs (hpoutclkx) should be terminated at the source with 22 Ω resistor as shown in Figure 7.

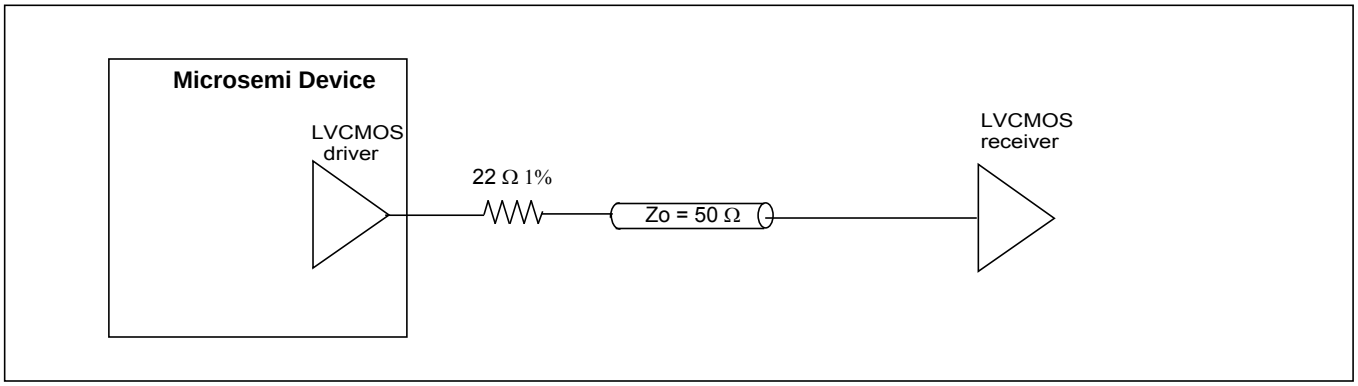


Figure 7 - Terminating LVCMOS outputs

4.8 Input Buffers

The ZL30162 has nine reference inputs ref[8:0]_p/ref[8:0]_n that can work as either single ended or differential and two references ref9 and ref10 that are only single ended input references. By default all reference inputs are single ended. This can be changed by programming **ref_config** register.

The input frequency range for differential inputs is: 1 Hz to 750 MHz; for single ended inputs is: 1 Hz to 177.5 MHz.

Differential reference inputs need to be properly terminated and biased as shown in Figure 8 and Figure 9 for LVPECL and Figure 10 and Figure 11 for LVDS drivers. When terminating LVPECL signal, it is necessary either to adjust termination resistors for DC coupling or to AC couple the LVPECL driver because ZL30162 differential inputs have different common mode (bias) voltage than LVPECL receivers. Thevenin termination (182 Ω and 68 Ω resistors) provide 50 ohm equivalent termination as well as biasing of the input buffer for DC coupled line. For AC coupled line, Thevenin termination with 127 Ω and 82 Ω resistors should be used as shown in Figure 9. The value of the AC coupling capacitors will depend on the minimum reference clock frequency. The value of 10 nF is good for input clock frequencies above 100 MHz. For lower clock frequencies capacitor values will have to be increased accordingly.

Terminations for DC and AC coupled LVDS line are shown in Figure 10 and Figure 11 respectively. Differential input biasing is provided by LVDS driver in case of DC coupling (Figure 10), whereas for AC coupling (Figure 11) biasing is generated by 12 kΩ and 8.2 kΩ resistors. In both cases, the line is terminated with 100 Ω resistor.

For single ended CMOS inputs, refx_n input needs to be connected to the ground as shown in Figure 12. The value of series termination resistor will depend on CMOS output driver but the most common values are 33 Ω and 22 Ω.

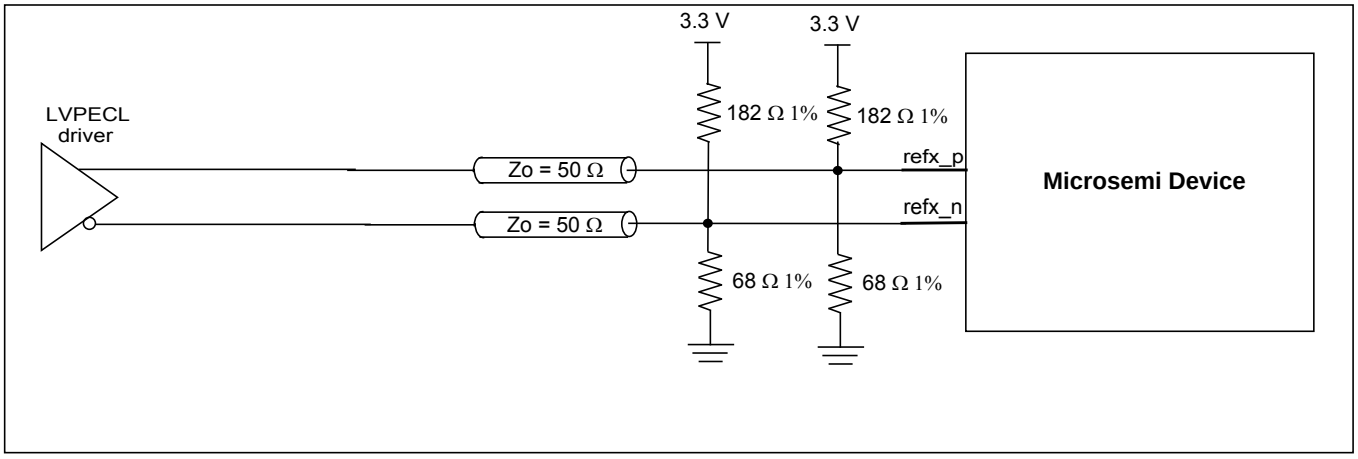


Figure 8 - Differential DC Coupled LVPECL Termination

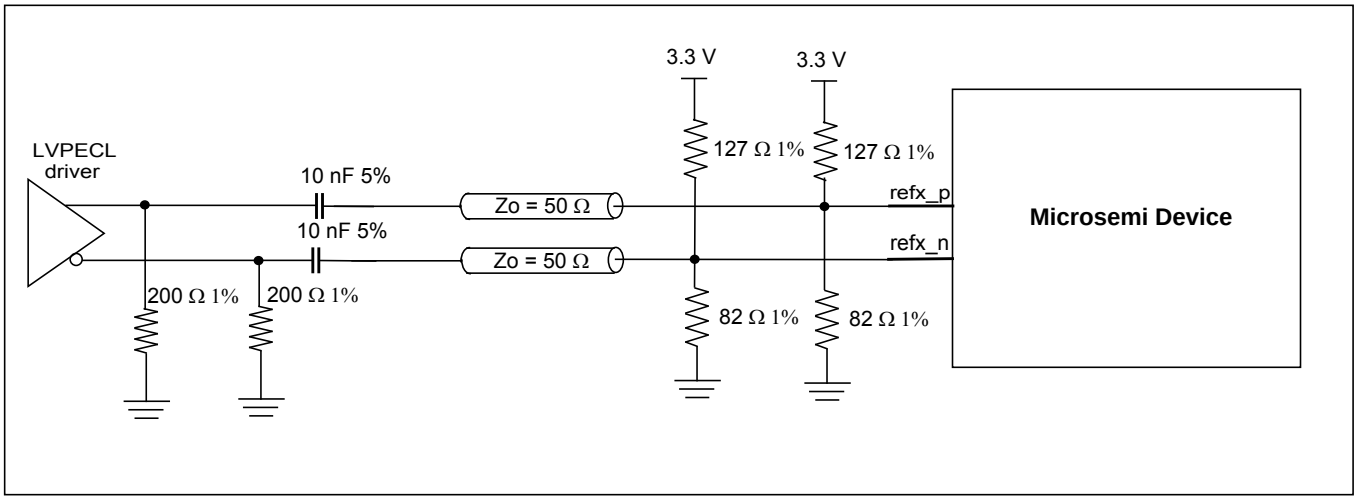


Figure 9 - Differential AC Coupled LVPECL Termination

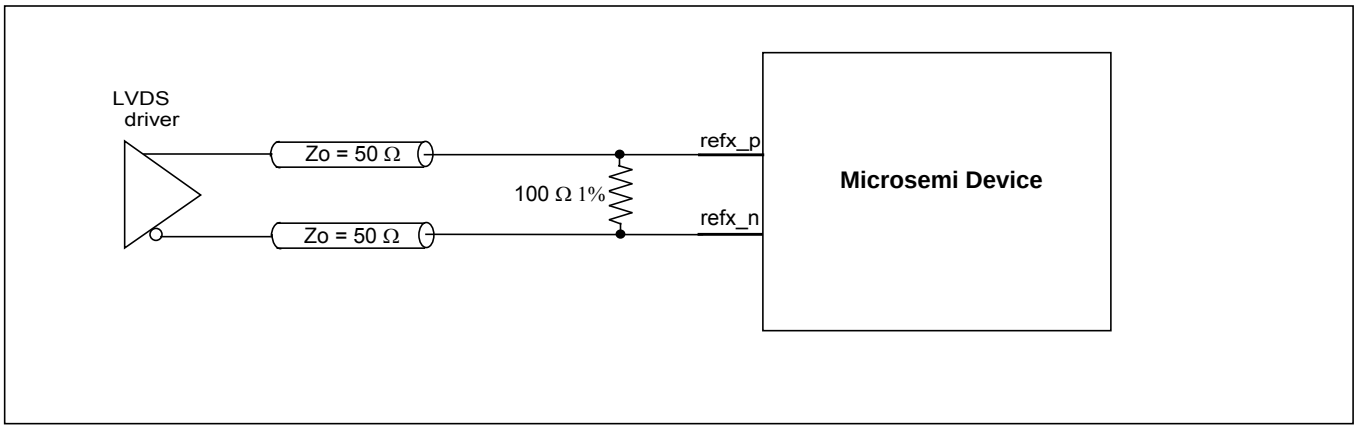


Figure 10 - Differential DC Coupled LVDS Termination

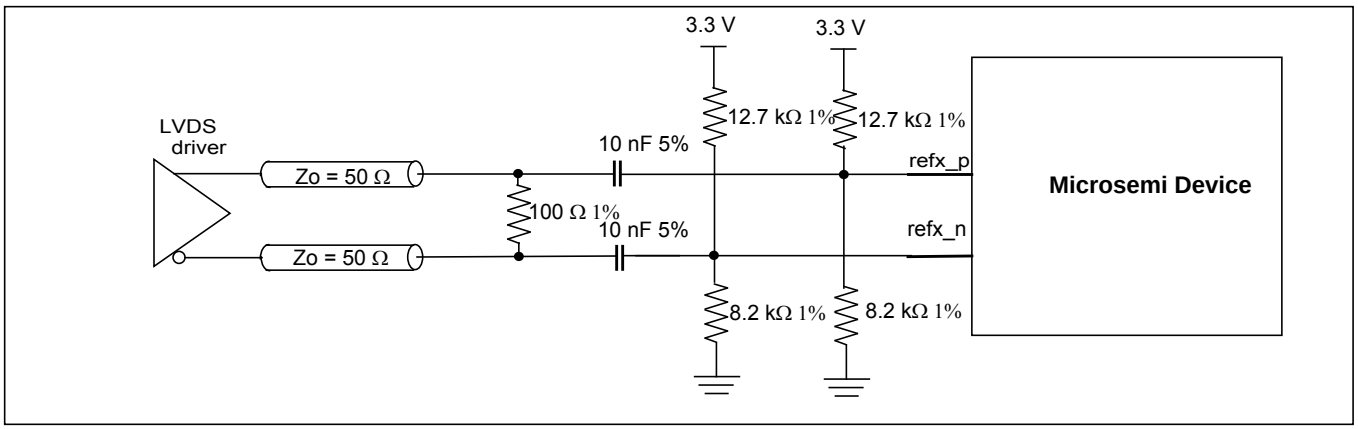


Figure 11 - Differential AC Coupled LVDS Termination

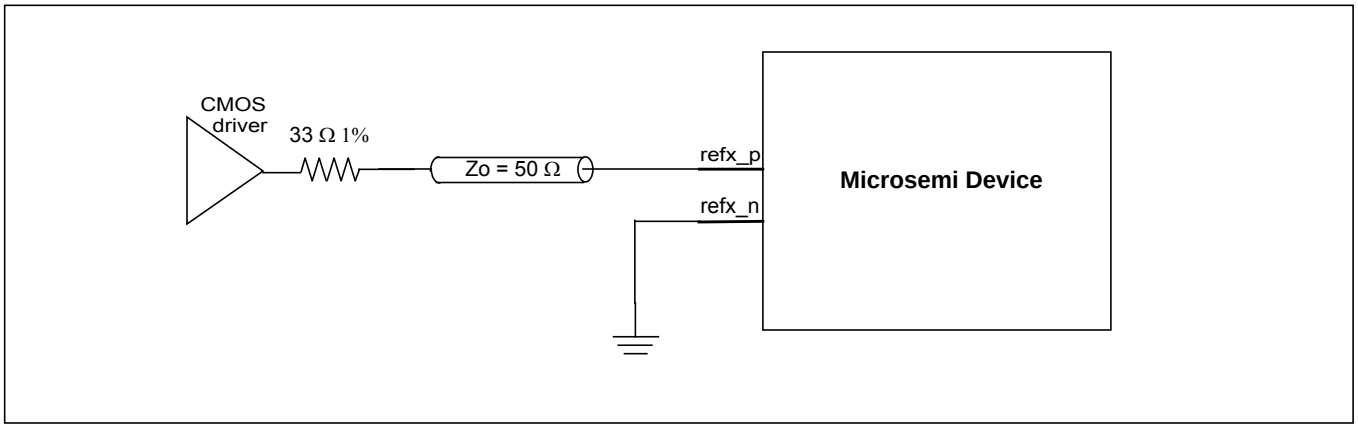


Figure 12 - Single Ended CMOS Termination

4.9 Master Clock Interface

The master oscillator determines the DPLL's free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL). Refer to the Application Note for a list of recommended clock oscillators.

4.10 Clock Oscillator

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **XOin** pin as shown in Figure 13. The connection to **XOin** should be direct and not AC coupled. The **osci_1V8** and **osci_3V3** pins must be grounded. The **osco_1V8** and **osco_3V3** pins must be left unconnected.

When using a crystal resonator as the master timing source, connect the crystal between **osci_1V8** and **osco_1V8** pins as shown in Figure 13. (While it is not preferred, the crystal can also be connected between the **osci_3V3** and **osco_3V3** pins.) The crystal should have bias resistor of 1 MΩ and load capacitances C1 and C2. Value of the load capacitances is dependent on the crystal and should be per the crystal's datasheet. The crystal should be a fundamental mode type -- not an overtone. When using 24.576 or 49.152 MHz oscillators, the user should maintain the default value of the **central_freq_offset** register (0x046AAAAB).

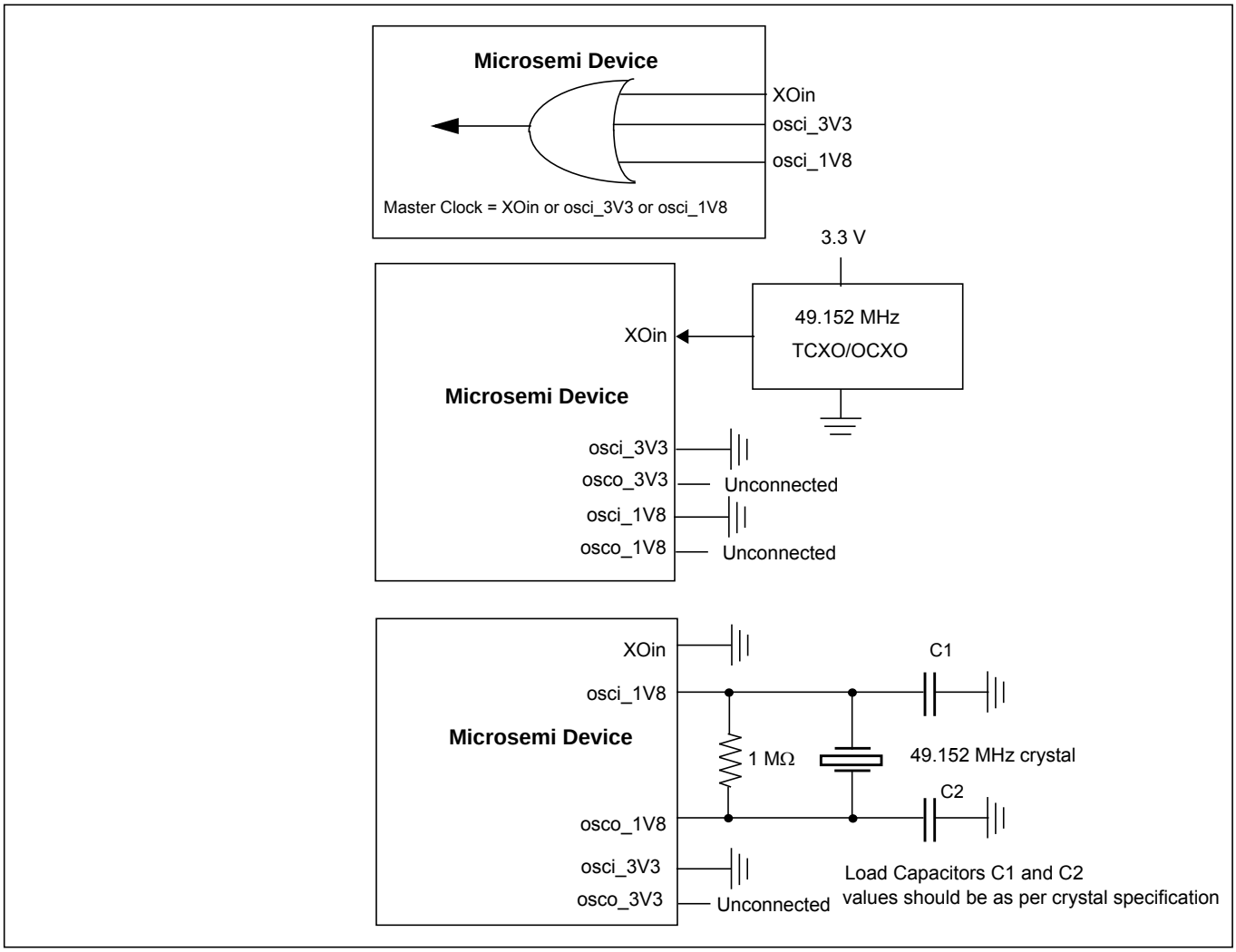


Figure 13 - Clock Oscillator Circuit

The device internal system clocks are generated off the device master clock input (oscillator or a crystal employing an on-chip buffer/driver). The master clock selection is done at start-up using the GPIO [1:0] pins, right after pwr_b gets de-asserted. The GPIO[1:0] pins are required to be in desired configuration (high or low) for 125 ms after the de-assertion of **pwr_b**, and then they can be released and used as regular GPIOs. Alternatively, these pins can be pulled high or low with 1 kΩ resistors.

GPIO [1:0]	Master Clock Frequency
00	24.576 MHz
01	49.152 MHz
10	20 MHz
11	reserved

Table 5 - Master Clock Frequency Selection

4.11 Power Up/Down Sequence

The 3.3 V supply should be powered before or simultaneously with the 1.8 V supply. The 1.8 V supply must never be greater than the 3.3 V supply by more than 0.3 V.

The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

4.12 Power Supply Filtering

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Microsemi Application Note ZLAN-327.

4.13 Reset and Configuration Circuit

To ensure proper operation, the device must be reset by holding the **pwr_b** pin low for at least 2 ms after power-up when 3.3V and 1.8V supplies are stable. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 14. This circuit provides approximately 2 ms of reset low time. The **pwr_b** input has a Schmidt trigger properties to prevent level bouncing.

Microsemi recommends that the power-on reset (**pwr_b**) signal be controlled by an on-board reset circuit or by a commercially available voltage supervisory device. It may also be possible to use a standalone power-up RC reset circuit. It is important to note that this circuit works reasonably well for power-up as long as the power supply rise time is fast with respect to the RC time constant, which may not always be the case. It is the board designer's responsibility to ensure that the circuit is properly tuned to each power supply's specific situation. As an example, for the capacitor C of 1 µF, the resistor should be 10 kΩ or higher.

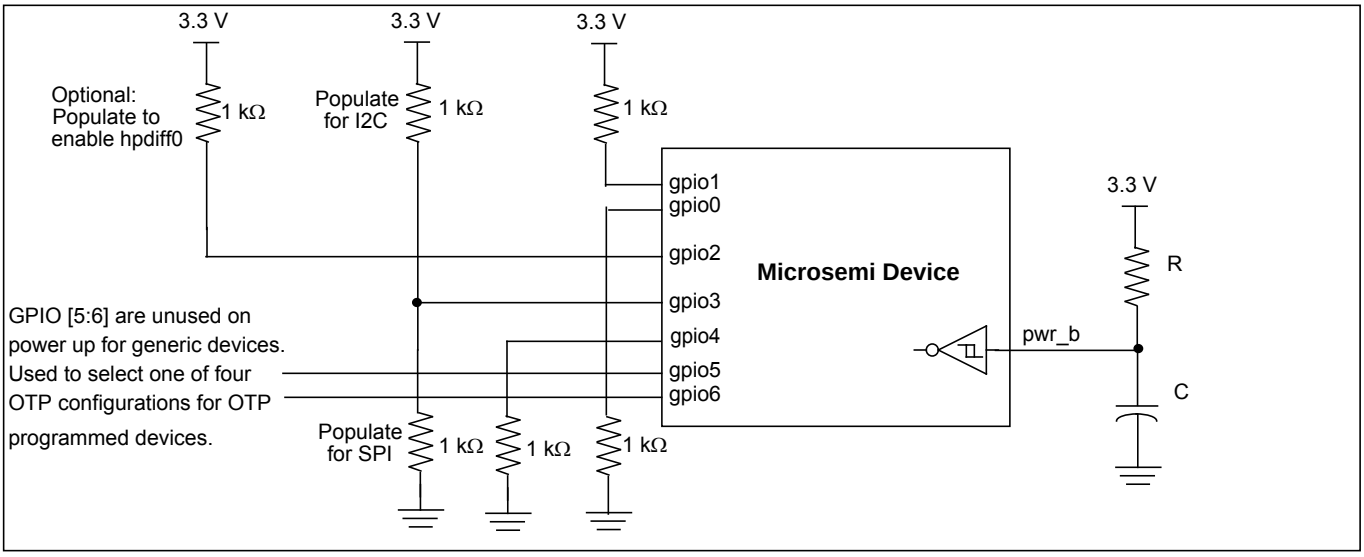


Figure 14 - Typical Power-Up Reset and Configuration Circuit

General purpose pins gpio[0,1,3,4,5,6] are used to configure device on power up. They have to be pulled up/down with 1 kΩ resistors as shown in Figure 14 or they can be held at the desired level for at least 125 ms after **pwr_b** goes high and then they can be released and used as general purpose I/O as described in Section 6.0.

By default all outputs are disabled to allow programing of required frequencies for different outputs and enabling corresponding outputs. During the prototype phase, hardware designer can verify if the device is working properly even before software driver is implemented just by pulling up gpio2 pin which enables hpdiff0 output (generates 622.08 MHz by default).

5.0 Configuration and Control

5.1 ZL30162 Configuration programming

The ZL30162 configuration is composed of 768 x 8 bits. The configuration registers are assigned their values by any one of the following three methods:

1. Default Configuration
2. Custom OTP (One Time Programmable) configuration
3. SPI/I2C configuration

5.1.1 Default Configuration

At power-up the device sets its configuration registers to the default values.

5.1.2 Custom OTP Configuration

At power-up the device sets its configuration registers to the defined custom configuration values stored in its one time programmable memory.
Custom configurations can be generated using Microsemi's ClockCenter+ GUI (ZLS30CCPLUS). Up to four unique custom configurations can be stored in the OTP memory and selected via GPIO pins 5,6 as follows:

GPIO 5	GPIO 6	Custom Configuration stored in slot
0	0	0
0	1	1
1	0	2
1	1	3

Table 6 - Custom Configuration power-up settings

For custom configured devices contact your local Microsemi Field Applications Engineer or Sales Manager.

5.1.3 SPI/I2C Configuration

The SPI/I2C host interface allows field programmability of the device's configuration registers. As an example, the user might start the device at nominal SONET rate, then switch to an FEC rate once the link's FEC rate is negotiated. Configurations set via the SPI/I2C interface are volatile and will need to be re-written if the device is reset or powered down.

5.2 Registers Configuration

This section refers to configuration registers that are set by the user to control operation of the device.

5.2.1 Input Reference Configuration

The following parameters can be configured for the reference input:

- Input reference frequency

- Default input reference selection
- Reference selection priority
- Automatic or manual reference switching
- Glitch-less or hit-less reference switching
- Reference switch based on single cycle monitor, coarse frequency monitor, guard soak timer and precise frequency monitor

5.2.2 DPLL Configuration

The following parameters can be configured for each DPLL:

- Input reference
- Loop bandwidth
- Phase slope limiter
- Pull-in range

5.2.3 Output Multiplexer Configuration

The following parameter can be configured:

- Select which DPLL drives which Synthesizer

5.2.4 Synthesizer Configuration

The following parameters can be configured for each Synthesizer:

- Synthesizers can be configured to be locked to any DPLL or disabled
- Synthesizer frequency between 1 GHz and 1.5 GHz

5.2.5 Output Dividers and Output Phase Offset (skew) Configuration

The following parameters can be configured:

- Output divider enable/disable
- Divider ratio
- Output phase offset (fine and coarse)

5.2.6 Output Drivers Configuration

The following parameters can be configured:

- Output enable/disable

5.3 GPIO Configuration

The device GPIO is configured using the SPI/I^2C. The following is an example of control inputs and status reporting outputs that can be accomplished using the GPIOs:

Status Outputs

- DPLL lock indicators
- DPLL holdover indicators

- Reference 0 to 10 fail indicators
- Interrupt

Control Inputs

- Select DPLL reference
- External Loss Of Signal (LOS) indications
- Enable/disable differential and single ended outputs
- Enable/disable TIE Clear
- Stop/start output clocks

The following table defines the functions of the GPIO pin when configured as a control input pin. Configuring the value in bit 6:0 in **gpio_function_pinX** register enables the desired function..

Value	Name	Description
Default		
0x00	Default	GPIO defined as an input. No function assigned.
Input References		
0x10	Ref0 external LOS signal	Ref0 external Loss Of Signal (LOS) - indicates to DPLLs that Ref0 has failed. This signal is used by DPLLs locked to Ref0 to do the reference switch or go to the holdover mode if another good reference is not available.
0x11	Ref1 external LOS signal	Same description as REF0 external LOS
0x12	Ref2 external LOS signal	Same description as REF0 external LOS
0x13	Ref3 external LOS signal	Same description as REF0 external LOS
0x14	Ref4 external LOS signal	Same description as REF0 external LOS
0x15	Ref5 external LOS signal	Same description as REF0 external LOS
0x16	Ref6 external LOS signal	Same description as REF0 external LOS
0x17	Ref7 external LOS signal	Same description as REF0 external LOS
0x18	Ref8 external LOS signal	Same description as REF0 external LOS
0x19	Ref9 external LOS signal	Same description as REF0 external LOS
0x1A	Ref10 external LOS signal	Same description as REF0 external LOS
TIE Clear		
0x20	DPLL0 Time Interval Error (TIE) clear enable	This signal is OR-ed with the 'DPLL0 TIE clear enable' bit of the **dpllX_ctrl** register. The functionality of this signal is explained in the **dpllX_ctrl** register.
0x28	DPLL1 Time Interval Error (TIE) clear enable	Same description as DPLL0 TIE clear enable
0x30	DPLL2 Time Interval Error (TIE) clear enable	Same description as DPLL0 TIE clear enable
0x38	DPLL3 Time Interval Error (TIE) clear enable	Same description as DPLL0 TIE clear enable

Value	Name	Description
Synthesizer Post Divider		
0x44	Stop output clock from Synthesizer0 Post Divider C bit1	This signal is OR-ed with the 'Synthesizer0 Post Divider C stop clock' bit1 in the **synth1_0_stop_clk** register.
0x45	Stop output clock from Synthesizer0 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x46	Stop output clock from Synthesizer0 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x47	Stop output clock from Synthesizer0 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4C	Stop output clock from Synthesizer1 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4D	Stop output clock from Synthesizer1 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4E	Stop output clock from Synthesizer1 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4F	Stop output clock from Synthesizer1 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x54	Stop output clock from Synthesizer2 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x55	Stop output clock from Synthesizer2 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x56	Stop output clock from Synthesizer2 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x57	Stop output clock from Synthesizer2 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5C	Stop output clock from Synthesizer3 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5D	Stop output clock from Synthesizer3 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5E	Stop output clock from Synthesizer3 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1

Value	Name	Description
0x5F	Stop output clock from Synthesizer3 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
High Performance Differential Outputs		
0x60	Enable Differential output HPDIFF0	This signal is OR-ed with the 'Enable HPDIFF0' bit in the **hp_diff_en** register. Functionality of this signal is explained in **hp_diff_en** register.
0x62	Enable Differential output HPDIFF1	Same description as Enable Differential output HPDIFF0
0x64	Enable Differential output HPDIFF2	Same description as Enable Differential output HPDIFF0
0x66	Enable Differential output HPDIFF3	Same description as Enable Differential output HPDIFF0
0x68	Enable Differential output HPDIFF4	Same description as Enable Differential output HPDIFF0
0x6A	Enable Differential output HPDIFF5	Same description as Enable Differential output HPDIFF0
0x6C	Enable Differential output HPDIFF6	Same description as Enable Differential output HPDIFF0
0x6E	Enable Differential output HPDIFF7	Same description as Enable Differential output HPDIFF0
High Performance CMOS Outputs		
0x70	Enable HPOUTCLK0	This signal is OR-ed with the 'Enable HPOUTCLK0' bit in the **hp_cmos_en** register.
0x72	Enable HPOUTCLK1	Same description as Enable HPOUTCLK0
0x74	Enable HPOUTCLK2	Same description as Enable HPOUTCLK0
0x76	Enable HPOUTCLK3	Same description as Enable HPOUTCLK0
0x78	Enable HPOUTCLK4	Same description as Enable HPOUTCLK0
0x7A	Enable HPOUTCLK5	Same description as Enable HPOUTCLK0
0x7C	Enable HPOUTCLK6	Same description as Enable HPOUTCLK0
0x7E	Enable HPOUTCLK7	Same description as Enable HPOUTCLK0

The following table defines the function of the GPIO pin when configured as a status output pin. Configuring the value in bit 6:0 in **gpio_function_pinX** registers enables the stated function.

Value	Name	Description
Interrupt		
0x80	Interrupt output signal	This bit will be high if the interrupt has been asserted.
Input Reference Status Indicators		
0x88	Ref0 - Precise Frequency Measurement (PFM) failure	This bit will be set if Ref0 PFM indicator is active (see **pfm_limit_refX** register for PFM limits).

Value	Name	Description
0x89	Ref0 Single Cycle Measurement (SCM) failure	This bit will be set if Ref0 SCM indicator is active (see **scm_cfm_limit_refX** register for SCM limits).
0x8A	Ref0 Coarse Frequency Measurement (CFM) failure	This bit will be set if Ref0 CFM indicator is active (see **scm_cfm_limit_refX** register for CFM limits).
0x8B	Ref0 Guard Soak Timer (GST) indicator	Ref0 Guard Soak Timer (GST) indicator
0x8C	Ref0 failure indicator	This bit will be set if either Ref0 external LOS signal is high, or Ref0 SCM, CFM or GST indicator is high, and appropriate mask bit in the 'Ref0 and Ref1 failure mask' register is set to 1 (not masked).
0x8D	Ref1 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0x8E	Ref1 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x8F	Ref1 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x90	Ref1 Guard Soak Timer (GST) indicator	Same description as for Ref0
0x91	Ref1 failure indicator	Same description as for Ref0
0x91	Ref2 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0x92	Ref2 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x94	Ref2 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x95	Ref2 Guard Soak Timer (GST) indicator	Same description as for Ref0
0x96	Ref2 failure indicator	Same description as for Ref0
0x97	Ref3 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0x98	Ref3 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x99	Ref3 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x9A	Ref3 Guard Soak Timer (GST) indicator	Same description as for Ref0
0x9B	Ref3 failure indicator	Same description as for Ref0
0x9C	Ref4 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0

Value	Name	Description
0x9D	Ref4 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x9E	Ref4 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x9F	Ref4 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xA0	Ref4 failure indicator	Same description as for Ref0
0xA1	Ref5 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0xA2	Ref5 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0xA3	Ref5 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0xA4	Ref5 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xA5	Ref5 failure indicator	Same description as for Ref0
0xA6	Ref6 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0xA7	Ref6 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0xA8	Ref6 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0xA9	Ref6 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xAA	Ref6 failure indicator	Same description as for Ref0
0xAB	Ref7 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0xAC	Ref7 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0xAD	Ref7 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0xAE	Ref7 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xAF	Ref7 failure indicator	Same description as for Ref0
0xB0	Ref8 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0xB1	Ref8 Single Cycle Measurement (SCM) failure	Same description as for Ref0

Value	Name	Description
0xB2	Ref8 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0xB3	Ref8 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xB4	Ref8 failure indicator	Same description as for Ref0
0xB5	Ref9 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0xB6	Ref9 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0xB7	Ref9 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0xB8	Ref9 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xB9	Ref9 failure indicator	Same description as for Ref0
0xBA	Ref10 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0xBB	Ref10 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0xBC	Ref10 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0xBD	Ref10 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xBE	Ref10 failure indicator	Same description as for Ref0
DPLL Status Indicators		
0xC0	DPLL0 Normal mode indicator	This bit will be set when DPLL0 is in normal locking mode (not holdover, not freerun)
0xC1	DPLL0 holdover mode indicator	This bit will be set when DPLL0 is in holdover mode

Value	Name	Description
0xC2	DPLL0 used reference bit3	This bit in combination with DPLL0 ref sel bit2, bit1 and bit0 represents DPLL0 selected reference. Selection: bit3 bit2 bit1 bit0 0 0 0 0 = Ref0 0 0 0 1 = Ref1 0 0 1 0 = Ref2 0 0 1 1 = Ref3 0 1 0 0 = Ref4 0 1 0 1 = Ref5 0 1 1 0 = Ref6 0 1 1 1 = Ref7 1 0 0 0 = Ref8 1 0 0 1 = Ref9 1 0 1 0 = Ref10
0xC3	DPLL0 used reference bit2	See bit3 description
0xC4	DPLL0 used reference bit1	See bit3 description
0xC5	DPLL0 used reference bit0	See bit3 description
0xC6	DPLL0 phase memory hit	This bit will be set when DPLL0 phase is beyond selected phase memory limit (specified in the **phasemem_limit_refX** register).
0xC7	DPLL0 frequency range hit	This bit will be set when DPLL0 frequency is beyond pull-in/hold-in range limit, specified in the **dpllX_pullin_holdin** register
0xC8	DPLL0 phase slope limit	This bit will be set when DPLL0 frequency is beyond phase slope limit, specified in the **dpllX_ctrl** register
0xC9	DPLL0 Lock Indication 0	This bit will be set when DPLL0 phase error is less than 36 us during 10 s period.
0xCA	DPLL0 Lock Indication 1	This bit will be set when DPLL0 phase error is less than 1us during 1s period.
0xCB	DPLL0 Lock Indication 2	This bit will be set when DPLL0 phase error is less than 10us during 1s period.
0xCC	DPLL0 Lock Indication 3	This bit will be set when DPLL0 phase error is less than 10us during 10s period.
0xD0	DPLL1 Normal mode indicator	Same description as for DPLL0
0xD1	DPLL1 holdover mode indicator	Same description as for DPLL0
0xD2	DPLL1 used reference bit3	Same description as for DPLL0
0xD3	DPLL1 used reference bit2	Same description as for DPLL0
0xD4	DPLL1 used reference bit1	Same description as for DPLL0
0xD5	DPLL1 used reference bit0	Same description as for DPLL0
0xD6	DPLL1 phase memory hit	Same description as for DPLL0
0xD7	DPLL1 frequency range hit	Same description as for DPLL0

Value	Name	Description
0xD9	DPLL1 Lock Indication 0	Same description as for DPLL0
0xDA	DPLL1 Lock Indication 1	Same description as for DPLL0
0xDB	DPLL1 Lock Indication 2	Same description as for DPLL0
0xDC	DPLL1 Lock Indication 3	Same description as for DPLL0
0xE0	DPLL2 Normal mode indicator	Same description as for DPLL0
0xE1	DPLL2 holdover mode indicator	Same description as for DPLL0
0xE2	DPLL2 used reference bit3	Same description as for DPLL0
0xE3	DPLL2 used reference bit2	Same description as for DPLL0
0xE4	DPLL2 used reference bit1	Same description as for DPLL0
0xE5	DPLL2 used reference bit0	Same description as for DPLL0
0xE6	DPLL2 phase memory hit	Same description as for DPLL0
0xE7	DPLL2 frequency range hit	Same description as for DPLL0
0xE8	DPLL2 phase slope limit	Same description as for DPLL0
0xE9	DPLL2 Lock Indication 0	Same description as for DPLL0
0xEA	DPLL2 Lock Indication 1	Same description as for DPLL0
0xEB	DPLL2 Lock Indication 2	Same description as for DPLL0
0xEC	DPLL2 Lock Indication 3	Same description as for DPLL0
0xF0	DPLL3 Normal mode indicator	Same description as for DPLL0
0xF1	DPLL3 holdover mode indicator	Same description as for DPLL0
0xF2	DPLL3 used reference bit3	Same description as for DPLL0
0xF3	DPLL3 used reference bit2	Same description as for DPLL0
0xF4	DPLL3 used reference bit1	Same description as for DPLL0
0xF5	DPLL3 used reference bit0	Same description as for DPLL0
0xF6	DPLL3 phase memory hit	Same description as for DPLL0
0xF7	DPLL3 frequency range hit	Same description as for DPLL0
0xF8	DPLL3 phase slope limit	Same description as for DPLL0
0xF9	DPLL3 Lock Indication 0	Same description as for DPLL0
0xFA	DPLL3 Lock Indication 1	Same description as for DPLL0
0xFB	DPLL3 Lock Indication 2	Same description as for DPLL0
0xFC	DPLL3 Lock Indication 3	Same description as for DPLL0

5.3.1 GPIO Indication and Control Functionality

The devices includes registers to control the GPIO pins directly using **gpio_in_6_0**, **gpio_out_6_0** and **gpio_out_en_6_0**. These registers are used with the **gpio_function_pin*x*** registers.

To read a GPIO:

- Set the **gpio_function_pin*x*** to 0x00 (control, no function assigned)
- Set the bit for the pin in **gpio_out_en_6_0** to 0
- Read the current GPIO value in **gpio_in_6_0**

To set a GPIO:

- Set the **gpio_function_pin*x*** to 0x00 (control, no function assigned)
- Set the bit for the pin in **gpio_out_en_6_0** to 1
- The value in **gpio_out_6_0** for the GPIO is driven on the GPIO pin

5.4 State Control and Reference Switch Modes

In un-managed mode of operation, the DPLL state (normal, freerun and holdover) and the selected reference is automatically set by the internal state machine of the device. It is based on availability of a valid reference and on the reference's selection priority.

In managed mode of operation, the DPLL state (normal, freerun and holdover) and the selected reference is manually set by the user.

The device allows for a smooth transition from in and out of the two modes of operation. Hence if the DPLL was in managed mode, for example locked to Ref2 reference and switched to un-managed mode of operation, then the state machine continues managing the DPLL, locked to the Ref2 and it will not force reference switching to any other reference unless a change in the Ref2 input conditions occurs that necessitate a change to an alternate input reference.

Each DPLL has its own independent state control and reference selection state machine.

5.4.1 Un-managed Mode

The un-managed mode combines the functionality of the normal state with automatic holdover and automatic reference switching. In this mode, transitioning from one mode to the other is controlled by the device internal state machine.

The on-chip state machine monitors the DPLL status bits, and based on the status information the state machine makes a decision to force holdover or to perform reference switch.

The reference switching state machine is based on the internal clock monitoring of each of the available input references and their priorities.

The state machine selects a reference source based on its priority value defined in a control register and the current availability of the reference. If all the references are available, the reference with the highest priority is selected; if this reference fails, the next highest priority reference is selected, and so on.

In un-managed mode, the state machine only reacts to reference failure indicators and performs reference switching anytime one of the following conditions takes place assuming they are not masked with their corresponding mask bits:

- LOS detected a failure and refswitch mask LOS is at logic “1”
- SCM detected a failure and refswitch mask SCM is at logic “1”
- CFM detected a failure and refswitch mask CFM is at logic “1"
- PFM detected a failure and refswitch mask PFM is at logic “1"
- GST is triggered and refswitch mask GST is at logic “1"

In un-managed mode, the device automatically selects a valid reference input. If the current reference used for synchronization fails, the state machine switches to another available reference. If all the available references fail, then the device enters the holdover mode under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and holdover mask LOS is at logic “1”
- SCM detected a failure and holdover mask SCM is at logic “1”
- CFM detected a failure and holdover mask CFM is at logic “1"
- PFM detected a failure and holdover mask PFM is at logic “1"
- GST is triggered and holdover mask GST is at logic “1"

In un-managed mode of operation, the state machine automatically recovers from holdover when the conditions to enter auto-holdover are not present.

The reference selection is based on reference priority. The current active reference for each DPLL can be read from DPLLx Reference Selection Status register.

Reference Priority

Every reference is assigned a priority value (0 to 10) to allow system designers to specify the priority of each input references. The priorities are relative to each other, with lower value numbers being the higher priority. value “1111" disables the ability to select the reference (i.e., don’t use for synchronization). If two or more inputs are given the same priority number, the input is selected based on the reference naming convention (i.e., ref0 is higher priority than ref1). The default reference selection priority is equal to its reference number (i.e., ref0 is highest priority and ref10 is the lowest priority).

When two references have the same priority they will not revert to each other (as reference availability change), but they will revert to a reference with a higher priority when it is available.

5.4.2 Managed (Manual) Mode

In managed mode, the device does not auto-select between different reference inputs. The user specifies which reference to use for synchronization and if it fails the DPLL enters the auto-holdover mode without switching to another reference.

The user (external uP) monitors the device status bits. Based on the status information, the user makes a decision to force holdover or to perform reference switch. In managed mode the active reference input is selected based on reference selection control bits. If the user sets the device to lock to a failed reference, the device stays in auto-holdover and only locks to that reference if it becomes valid.

The state machine only reacts to failure indicators and goes into auto-holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and holdover mask LOS is at logic “1”
- SCM detected a failure and holdover mask SCM is at logic “1”
- CFM detected a failure and holdover mask CFM is at logic “1"
- PFM detected a failure and holdover mask PFM is at logic “1"
- GST is triggered and holdover mask GST is at logic “1"

The state machine automatically recovers from auto-holdover when the conditions to enter auto-holdover are not present.

Time critical transitions for entry into auto-holdover and exit from auto-holdover are managed by the internal state machine. A change of the reference select bits triggers an internal state transition into auto-holdover and then an exit into Normal state and locking to the new reference.

5.5 Reference/Sync Pairing

This device allows any input reference be fed with sync (frame pulse) or clock. A sync input reference is selected by the DPLL with the main reference and is used to control the phase of the output frame pulse. (When used as a sync input, it is important to remove this reference from any automatic reference selection as explained in 5.4.1, “Un-managed Mode“.) An example of output frame pulse alignment is shown in Figure 15.

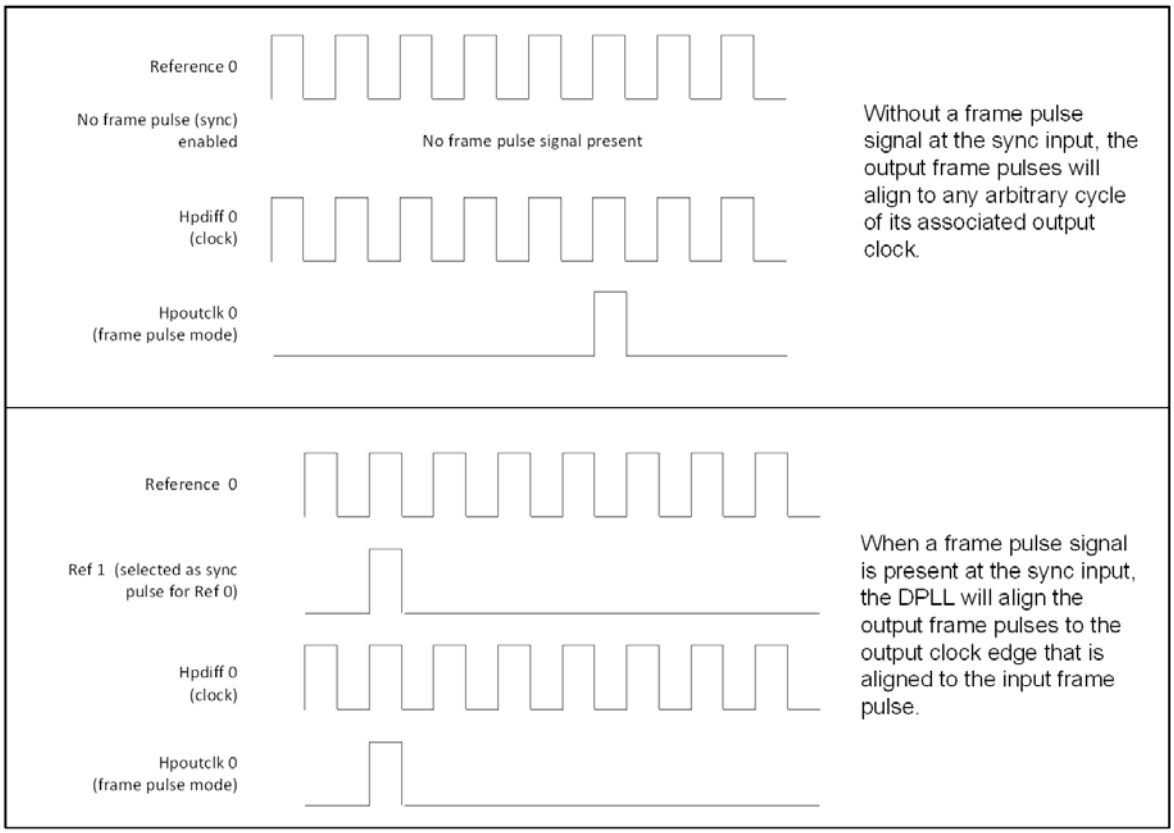


Figure 15 - Output Frame Pulse Alignment

In this example, the reference is on ref0 and the sync pulse is on ref1. The ouptut clock is on hpdiff0 and the output frame pulse is on hpclk0. Any pair of reference can be used for ref/sync pairing, but the output clock and output frame pulse must be on the same synthesizer. The DPLL selects the reference and the sync pulse (if provisioned) is used automatically.

Provisioning the reference and frame pulse (sync) input can be done through the GUI or via registers. For example, the register **ref_1_0_clk_sync_pair** is used to select the corresponding sync pulse for references 0 and 1. When the pair for a reference it set to itself, this feature is disabled.

6.0 Host Interface

A host processor controls and receives status from the Microsemi device using either a SPI or an I^2C interface.

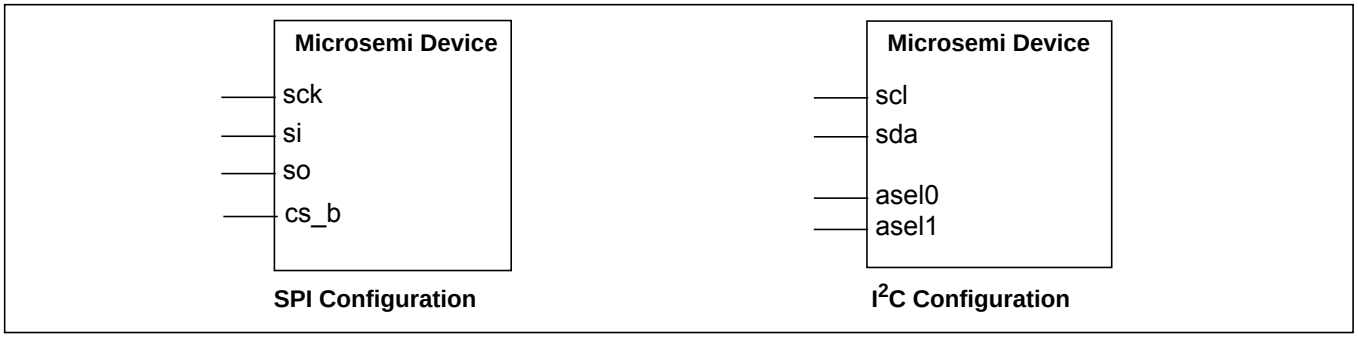


Figure 16 - Serial Interface Configuration

The selection between I^2C and SPI interfaces is performed at start-up using GPIO[3] pin, as **pwr_b** gets de-asserted. The GPIO[3] pin needs to be held at required level for 125 ms after the de-assertion of **pwr_b**, after which time they can be released and used as regular GPIO.

GPIO[3]	Serial Interface
0	SPI
1	I2C

Table 7 - Serial Interface Selection

Both interfaces use seven bit address field and the device has eight bit address space. Hence, the device register space is divided in five pages of 127 register each. Page 0 has addresses 0x000 to 0x07E and Page 1 with addresses 0x080 to 0x0FF and so on until page 5 which has addresses 0x200 to 0x27E. The host selects between the pages by writing to the Page Select register (address 0x7F on each page). e.g. writing a 0x03 to the page select register makes registers 0x180 to 0x1FF available through the host interface.

6.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the device internal registers that are used to configure, read status, and allow manual control of the device.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **so**_asel1 pin must be ignored. Similarly, the input data on the **si**_sda pin is ignored by the device during a read cycle.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission or Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **sck**_scl pin when the **cs**_**b**_asel0 pin is active. If the **sck**_scl pin is low during **cs**_**b**_asel0 activation, then MSb first timing is selected. If the **sck**_scl pin is high during **cs**_**b**_asel0 activation, then LSb first timing is assumed.

The SPI port expects 1-bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **cs**_**b**_asel0 pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal **cs**_**b**_asel0 is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

Functional waveforms for the LSb and MSb first mode, and burst mode are shown in Figure 17, Figure 18 and Figure 19. Timing characteristics are shown in Table 9, Figure 32, and Figure 33.

6.1.1 Least Significant Bit (LSb) First Transmission Mode

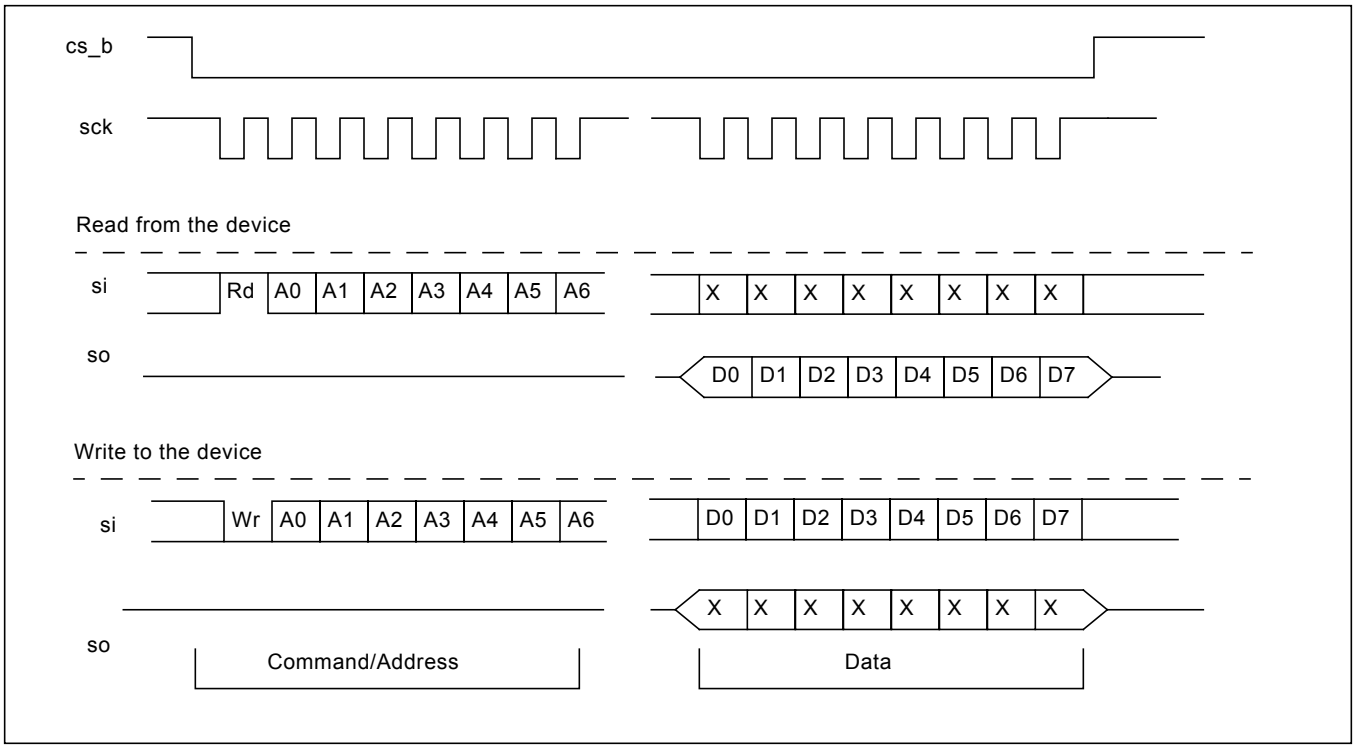


Figure 17 - Serial Peripheral Interface Functional Waveforms - LSb First Mode

6.1.2 Most Significant Bit (MSb) First Transmission Mode

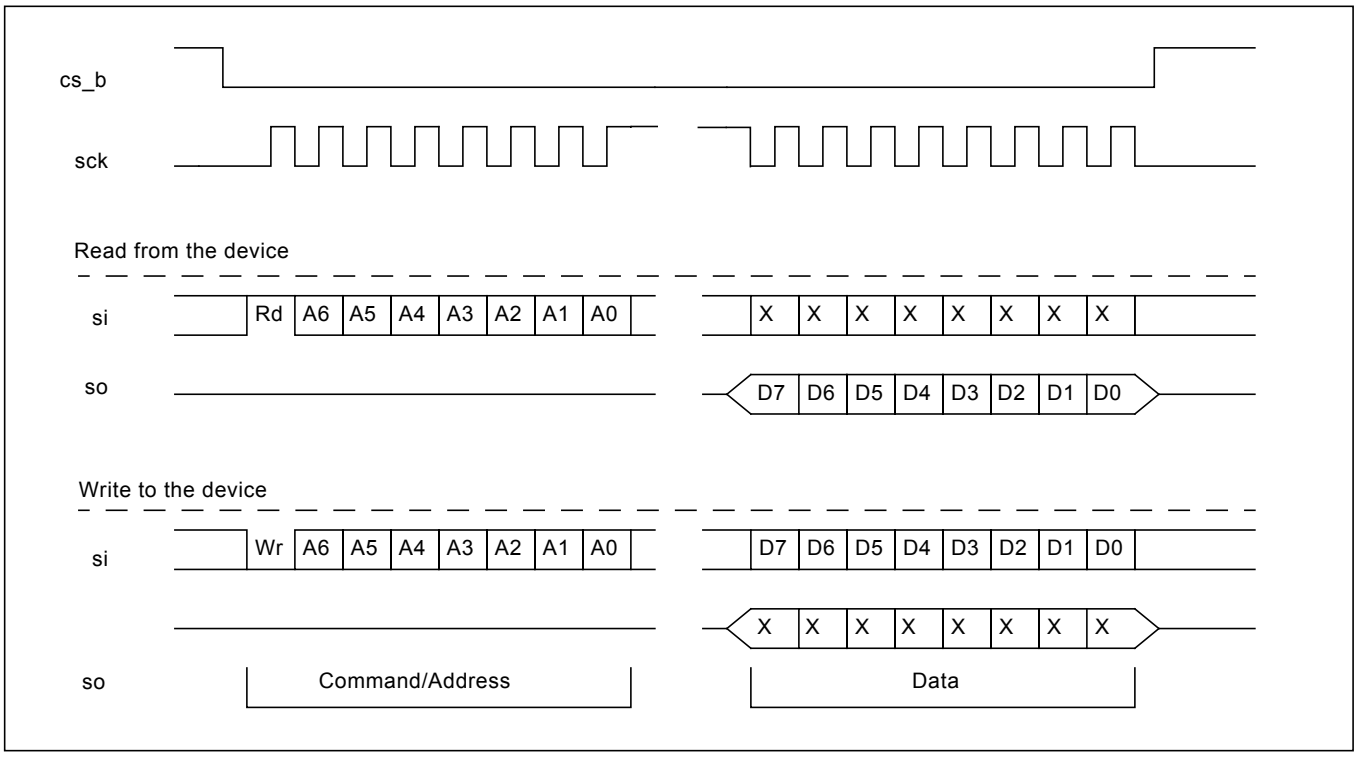


Figure 18 - Serial Peripheral Interface Functional Waveforms - MSb First Mode

6.1.3 SPI Burst Mode Operation

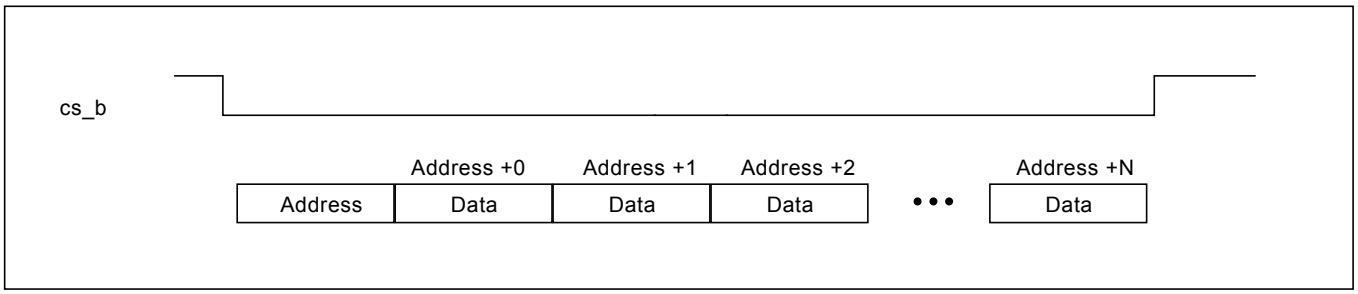


Figure 19 - Example of a Burst Mode Operation

6.2 I^2C Interface

The I^2C controller supports version 2.1 (January 2000) of the Philips I^2C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) mode. Burst mode is supported in both standard and fast modes.

Data is transferred MSb first and occurs in 1 byte blocks. As shown in Figure 20, a write command consists of a 7-bit device (slave) address, a R/W indicator bit, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

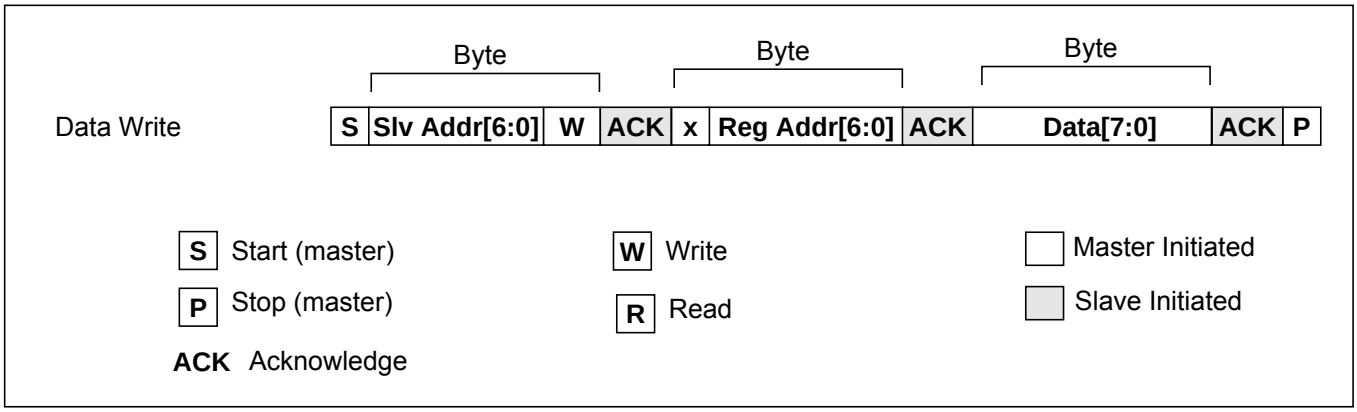


Figure 20 - I²C Data Write Protocol

A read is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in Figure 21.

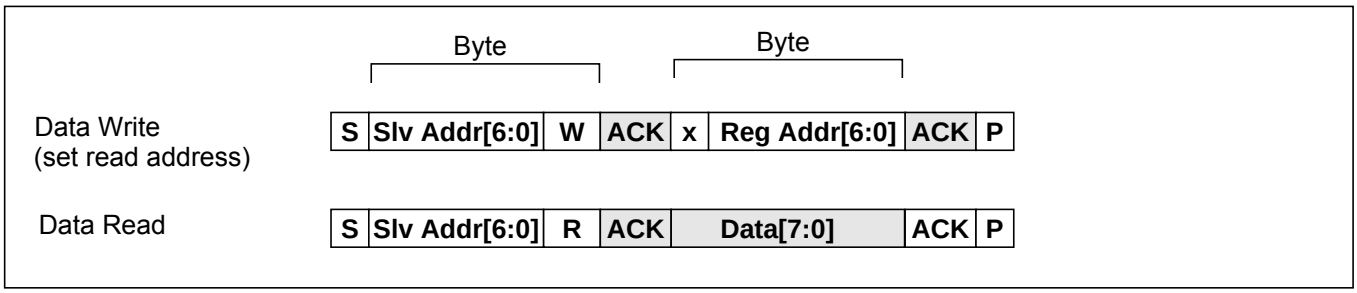


Figure 21 - I²C Data Read Protocol

The 7-bit device (slave) address contains a 5-bit fixed address plus variable bits which are set with the **asel0,** and **asel1** pins. This allows multiple ZL30162s to share the same I²C bus. The address configuration is shown in Figure 22.

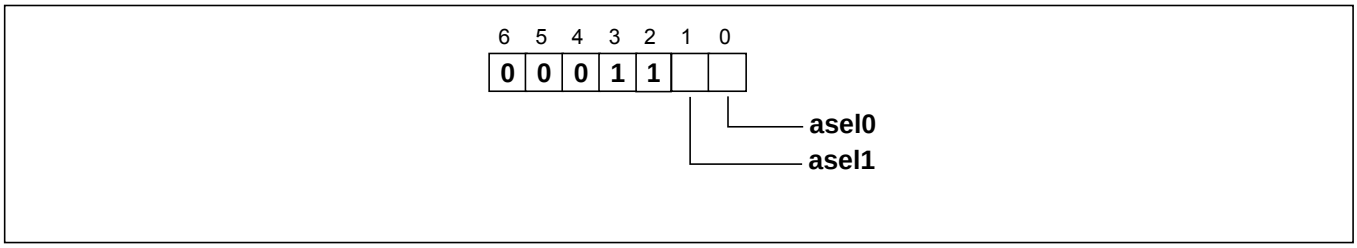


Figure 22 - I²C 7-bit Slave Address

The device also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 23 (write) and Figure 24 (read). The first data byte is written/read to/from the specified address, and subsequent data bytes are written/read using an automatically increment address. The maximum auto increment address of a burst operation is 0x7F and operations beyond this limit will be ignored. In other words, the auto increment address does not wrap around to 0x00 after reaching 0x7F.

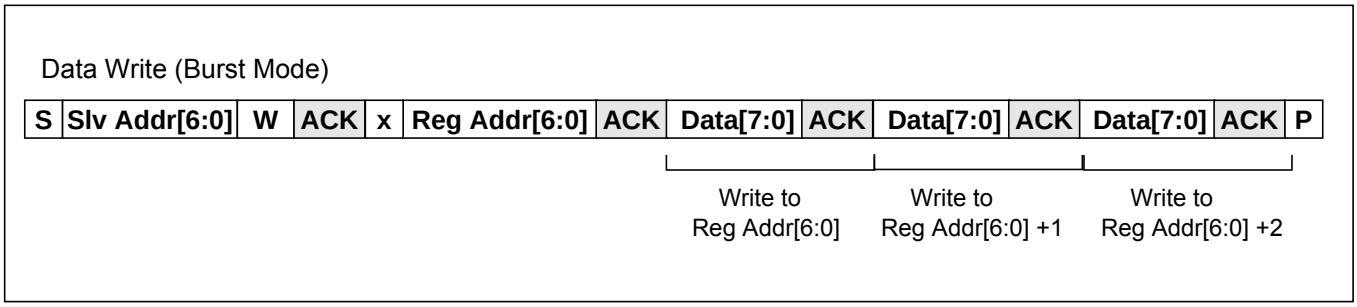


Figure 23 - I²C Data Write Burst Mode

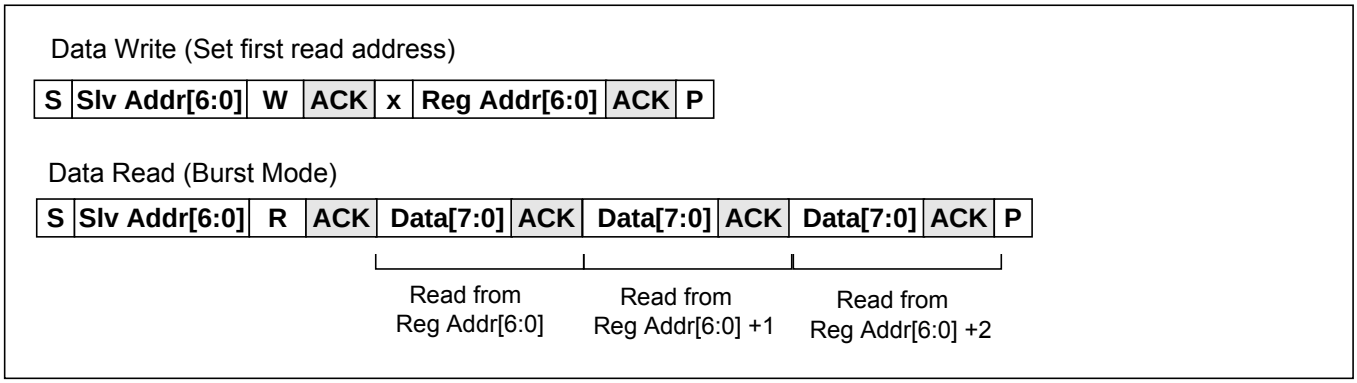


Figure 24 - I²C Data Read Burst Mode

7.0 Register Map

The device is controlled by accessing registers through the serial interface (SPI or I^2C). The device can be configured to operate in un-managed (automatic) mode which minimizes its interaction with the system's processor, or it can operate in a managed (manual) mode where the system processor controls operation of the device.

A simple way to generate configuration for the device is to use the evaluation board GUI which can operate standalone (without the evaluation board). Through the GUI the user can quickly set all required parameters and save the configuration to a text file which can then be used by the system processor to load and configure the device.

Multi-byte Register Values

The device register map is based on 8-bit register access, so register values that require more than 8 bits are spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order. The 8-bit register containing the most significant byte (MSB) must be accessed first, and the register containing the least significant byte (LSB) must be accessed last. An example of a multi-byte register is shown in Figure 25. When writing a multi-byte value, the value is latched when the LSB is written.

Example:
The input reference M and N 16 are bit values defining the M/N ratio is programmed using a 32-bit value which is spread over four 8-bit registers. The MSB is contained in address 0x1BC and the LSB in 0x1BF When reading or writing this multi-byte value, the MSB must be accessed first, then the middle bytes, and the LSB last.

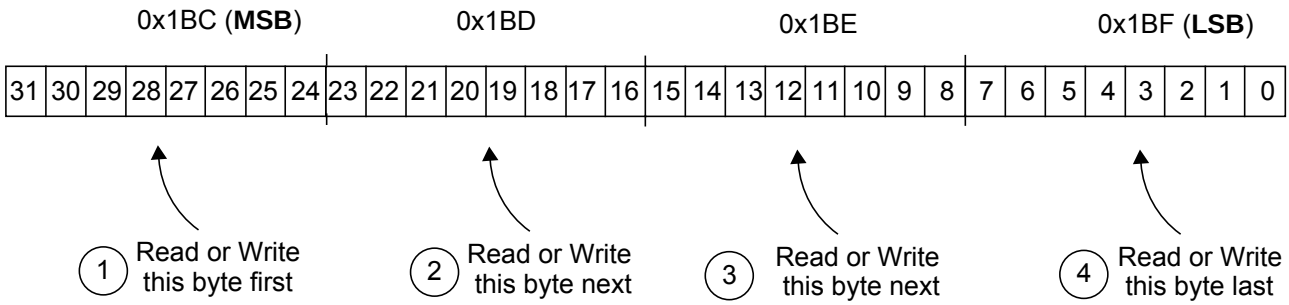


Figure 25 - Accessing Multi-byte Register Values

Time between two write accesses to the same register

- User should wait at least 25 ms between two write accesses to the same register
  - The **dpll*n*_df_offset** registers can be written with a minimum wait time of 300 microseconds between write accesses to the same register.
- For the page selection register (at addresses 0x07F, 0x0FF, 0x17F, 0x1FF, 0x27F and 0x2FF), there is no waiting time required between write accesses.

Basic Procedure for Refreshing Latest Device Status from Sticky Read (StickyR) Registers without Interrupt Handler

Access to some status registers is defined as Sticky Read (StickyR). Procedure for accessing these registers is:

-write 0x01 to Sticky Lock Register at address 0x011

-clear status register(s) by writing 0x00 to it

-write 0x00 to StickyR Lock Register at address 0x011

-wait for 25 ms

-read the status register(s)

Basic Procedure for Refreshing Latest Device Status from Sticky Read (StickyR) Registers when using an Interrupt Handler (event or polling)

Access to some status registers is defined as Sticky Read (StickyR). Procedure for accessing these registers is:

-host receives IRQ event or poll timer expiry

-disable the CPU IRQ

-write 0x01 to Sticky Lock Register at address 0x011

-read status register(s) (Sticky Status since the last IRQ)

-clear status register(s) by writing 0x00 to it

-write 0x00 to StickyR Lock Register at address 0x011

-exit IRQ handler or IRQ poll routine

-Re-enable the CPU IRQ

-next update to status will not occur for for another 25 ms

-wait for IRQ event or poll timer expiry

The following table provides a summary of the registers available for status and configuration of the device.Devices with a custom OTP configuration will power-up with the custom configuration values instead of the default values.

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
Miscellaneous Registers				
0x000	ready	0x1F	Ready Indicator register	R
0x001	id_reg	0xA2	Chip ID Register	R
0x002	hw_rev_reg	0x05	Chip Hardware Revision register	R
0x00B:0x00E	central_freq_offset	0x046AAAAB	Central frequency offset	R/W
0x010	spurs_supression	0x00	Spurs supression	R/W
0x011	sticky_lock	0x00	Sticky Lock Register	R/W
Input Reference Monitoring and DPLL Status				
0x020	ref_fail_isr_status_7_0	0x00	Reference failure interrupt status register for Ref 7:0	StickyR/W
0x021	ref_fail_isr_status_10_8	0x00	Reference failure interrupt status register for Ref 10:8	StickyR/W
0x022	dpll_isr_status	0x00	DPLL interrupt status register	StickyR/W
0x023	ref_fail_isr_mask_7_0	0x00	Reference failure interrupt mask register fro Ref 7:0	R/W
0x024	ref_fail_isr_mask_10_8	0x00	Reference failure interrupt mask register fro Ref 10:8	R/W
0x025	dpll_isr_mask	0x00	DPLL interrupt status register	R/W
0x026	ref_mon_fail_0	0x00	Reference 0 Failure Indicators	StickyR/W
0x027	ref_mon_fail_1	0x00	Reference 1 Failure Indicators	StickyR/W
0x028	ref_mon_fail_2	0x00	Reference 2 Failure Indicators	StickyR/W
0x029	ref_mon_fail_3	0x00	Reference 3 Failure Indicators	StickyR/W
0x02A	ref_mon_fail_4	0x00	Reference 4 Failure Indicators	StickyR/W
0x02B	ref_mon_fail_5	0x00	Reference 5 Failure Indicators	StickyR/W
0x02C	ref_mon_fail_6	0x00	Reference 6 Failure Indicators	StickyR/W
0x02D	ref_mon_fail_7	0x00	Reference 7 Failure Indicators	StickyR/W
0x02E	ref_mon_fail_8	0x00	Reference 8 Failure Indicators	StickyR/W
0x02F	ref_mon_fail_9	0x00	Reference 9 Failure Indicators	StickyR/W
0x030	ref_mon_fail_10	0x00	Reference 10 Failure Indicators	StickyR/W

Table 8 - Register Map

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x036	ref_mon_fail_mask_0	0x16	Reference 0 Failure Masks	R/W
0x037	ref_mon_fail_mask_1	0x16	Reference 1 Failure Masks	R/W
0x038	ref_mon_fail_mask_2	0x16	Reference 2 Failure Masks	R/W
0x039	ref_mon_fail_mask_3	0x16	Reference 3 Failure Masks	R/W
0x03A	ref_mon_fail_mask_4	0x16	Reference 4 Failure Masks	R/W
0x03B	ref_mon_fail_mask_5	0x16	Reference 5 Failure Masks	R/W
0x03C	ref_mon_fail_mask_6	0x16	Reference 6 Failure Masks	R/W
0x03D	ref_mon_fail_mask_7	0x16	Reference 7 Failure Masks	R/W
0x03E	ref_mon_fail_mask_8	0x16	Reference 8 Failure Masks	R/W
0x03F	ref_mon_fail_mask_9	0x16	Reference 9 Failure Masks	R/W
0x040	ref_mon_fail_mask_10	0x16	Reference 10 Failure Masks	R/W
0x046	gst_disqualif_time_3_0	0xAA	Guard soak timer (GST) disqualify time selection for Ref3:0	R/W
0x047	gst_disqualif_time_7_4	0xAA	Guard soak timer (GST) disqualify time selection for Ref7:4	R/W
0x048	gst_disqualif_time_10_8	0x2A	Guard soak timer (GST) disqualify time selection for Ref10:8	R/W
0x04A	gst_qualif_time_3_0	0x55	Guard soak timer (GST) qualify time selection for Ref 3:0	R/W
0x04B	gst_qualif_time_7_4	0x55	Guard soak timer (GST) qualify time selection for Ref 7:4	R/W
0x04C	gst_qualif_time_10_8	0x15	Guard soak timer (GST) qualify time selection for Ref 10:8	R/W
0x050	scm_cfm_limit_ref0	0x55	SCM and CFM limits for Reference 0	R/W
0x051	scm_cfm_limit_ref1	0x55	SCM and CFM limits for Reference 1	R/W
0x052	scm_cfm_limit_ref2	0x55	SCM and CFM limits for Reference 2	R/W
0x053	scm_cfm_limit_ref3	0x55	SCM and CFM limits for Reference 3	R/W
0x054	scm_cfm_limit_ref4	0x55	SCM and CFM limits for Reference 4	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x055	scm_cfm_limit_ref5	0x55	SCM and CFM limits for Reference 5	R/W
0x056	scm_cfm_limit_ref6	0x55	SCM and CFM limits for Reference 6	R/W
0x057	scm_cfm_limit_ref7	0x55	SCM and CFM limits for Reference 7	R/W
0x058	scm_cfm_limit_ref8	0x55	SCM and CFM limits for Reference 8	R/W
0x059	scm_cfm_limit_ref9	0x55	SCM and CFM limits for Reference 9	R/W
0x05A	scm_cfm_limit_ref10	0x55	SCM and CFM limits for Reference 10	R/W
0x060	pfm_limit_ref1_0	0x33	PFM limits for References 1 and 0	R/W
0x061	pfm_limit_ref3_2	0x33	PFM limits for References 3 and 2	R/W
0x062	pfm_limit_ref5_4	0x33	PFM limits for References 5 and 4	R/W
0x063	pfm_limit_ref7_6	0x33	PFM limits for Reference 7 and 6	R/W
0x064	pfm_limit_ref9_8	0x33	PFM limits for Reference 9 and 8	R/W
0x065	pfm_limit_ref10	0x03	PFM limits for Reference 10	R/W
0x068	phase_acq_en_7_0	0xFF	Phase Acquisition enable for Acq7:0	R/W
0x069	phase_acq_en_10_8	0x07	Phase Acquisition enable for Acq10:8	R/W
0x06A	phasemem_limit_ref0	0x1B	Phase memory limit for Reference 0	R/W
0x06B	phasemem_limit_ref1	0x1B	Phase memory limit for Reference 1	R/W
0x06C	phasemem_limit_ref2	0x1B	Phase memory limit for Reference 2	R/W
0x06D	phasemem_limit_ref3	0x1B	Phase memory limit for Reference 3	R/W
0x06E	phasemem_limit_ref4	0x1B	Phase memory limit for Reference 4	R/W
0x06F	phasemem_limit_ref5	0x1B	Phase memory limit for Reference 5	R/W
0x070	phasemem_limit_ref6	0x1B	Phase memory limit for Reference 6	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x071	phasemem_limit_ref7	0x1B	Phase memory limit for Reference 7	R/W
0x072	phasemem_limit_ref8	0x1B	Phase memory limit for Reference 8	R/W
0x073	phasemem_limit_ref9	0x1B	Phase memory limit for Reference 9	R/W
0x074	phasemem_limit_ref10	0x1B	Phase memory limit for Reference 10	R/W
0x07A	ref_config_7_0	0x00	Reference configuration register for References 7 to 0	R/W
0x07B	ref_config_8	0x00	Reference configuration register for Reference 8	R/W
0x07C	ref_pre_divide_7_0	0x00	Reference predivider control register for Ref7:0	R/W
0x07D	ref_pre_divide_10_8	0x00	Reference predivider control register for Ref10:8	R/W
0x07F	page_sel_register	0x00	SPI Page Selection Register	R/W
Input Frequency Configuration				
0x080:0x081	ref0_base_freq	0x9C40	Ref0 base frequency Br0	R/W
0x082:0x083	ref0_freq_multiple	0x0F30	Ref0 base frequency multiple Kr0	R/W
0x084:0x087	ref0_ratio_M_N	0x00010001	Ref0 Forward Error Correction (FEC) multiplication ratio Mr0 / Nr0 (numerator Mr0 and denominator Nr0 values)	R/W
0x088:0x089	ref1_base_freq	0x9C40	Ref1 base frequency Br1	R/W
0x08A:0x08B	ref1_freq_multiple	0x01E6	Ref1 base frequency multiple Kr1	R/W
0x08C:0x08F	ref1_ratio_M/N	0x00010001	Ref1 Forward Error Correction (FEC) multiplication ratio Mr1/ Nr1	R/W
0x090:0x091	ref2_base_freq	0x9C40	Ref2 base frequency Br2	R/W
0x092:0x093	ref2_freq_multiple	0x01E6	Ref2 base frequency multiple Kr2	R/W
0x094:0x097	ref2_ratio_M/N	0x00010001	Ref2 Forward Error Correction (FEC) multiplication ratio Mr2 / Nr2	R/W
0x098:0x099	ref3_base_freq	0x9C40	Ref3 base frequency Br3	R/W
0x09A:0x09B	ref3_freq_multiple	0x01E6	Ref3 base frequency multiple Kr3	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x09C:0x09F	ref3_ratio_M/N	0x00010001	Ref3 Forward Error Correction (FEC) multiplication ratio Mr3 / Nr3	R/W
0x0A0:0x0A1	ref4_base_freq	0x9C40	Ref4 base frequency Br4	R/W
0x0A2:0x0A3	ref4_freq_multiple	0x01E6	Ref4 base frequency multiple Kr4	R/W
0x0A4:0x0A7	ref4_ratio_M/N	0x00010001	Ref4 Forward Error Correction (FEC) multiplication ratio Mr4 / Nr4	R/W
0x0A8:0x0A9	ref5_base_freq	0x9C40	Ref5 base frequency Br5	R/W
0x0AA:0x0AB	ref5_freq_multiple	0x01E6	Ref5 base frequency multiple Kr5	R/W
0x0AC:0x0AF	ref5_ratio_M/N	0x00010001	Ref5 Forward Error Correction (FEC) multiplication ratio Mr5 / Nr5	R/W
0x0B0:0x0B1	ref6_base_freq	0x9C40	Ref6 base frequency Br6	R/W
0x0B2:0x0B3	ref6_freq_multiple	0x01E6	Ref6 base frequency multiple Kr6	R/W
0x0B4:0x0B7	ref6_ratio_M/N	0x00010001	Ref6 Forward Error Correction (FEC) multiplication ratio Mr6 / Nr6	R/W
0x0B8:0x0B9	ref7_base_freq	0x9C40	Ref7 base frequency Br7	R/W
0x0BA:0x0BB	ref7_freq_multiple	0x01E6	Ref7 base frequency multiple Kr7	R/W
0x0BC:0x0BF	ref7_ratio_M/N	0x00010001	Ref7 Forward Error Correction (FEC) multiplication ratio Mr7 / Nr7	R/W
0x0C0:0x0C1	ref8_base_freq	0x9C40	Ref8 base frequency Br8	R/W
0x0C2:0x0C3	ref8_freq_multiple	0x01E6	Ref8 base frequency multiple Kr8	R/W
0x0C4:0x0C7	ref8_ratio_M/N	0x00010001	Ref8 Forward Error Correction (FEC) multiplication ratio Mr8 / Nr8	R/W
0x0C8:0x0C9	ref9_base_freq	0x9C40	Ref9 base frequency Br9	R/W
0x0CA:0x0CB	ref9_freq_multiple	0x01E6	Ref9 base frequency multiple Kr9	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x0CC:0x0CF	ref9_ratio_M/N	0x00010001	Ref9 Forward Error Correction (FEC) multiplication ratio Mr9 / Nr9	R/W
0x0D0:0x0D1	ref10_base_freq	0x9C40	Ref10 base frequency Br10	R/W
0x0D2:0x0D3	ref10_freq_multiple	0x01E6	Ref10 base frequency multiple Kr10	R/W
0x0D4:0x0D7	ref10_ratio_M/N	0x00010001	Ref10 Forward Error Correction (FEC) multiplication ratio Mr10 / Nr10	R/W
0x0D8	ref0_sync_misc_ctrl	0x00	Ref0 sync miscellaneous control	R/W
0x0D9	ref1_sync_misc_ctrl	0x00	Ref1 sync miscellaneous control	R/W
0x0DA	ref2_sync_misc_ctrl	0x00	Ref2 sync miscellaneous control	R/W
0x0DB	ref3_sync_misc_ctrl	0x00	Ref3 sync miscellaneous control	R/W
0x0DC	ref4_sync_misc_ctrl	0x00	Ref4 sync miscellaneous control	R/W
0x0DD	ref5_sync_misc_ctrl	0x00	Ref5 sync miscellaneous control	R/W
0x0DE	ref6_sync_misc_ctrl	0x00	Ref6 sync miscellaneous control	R/W
0x0DF	ref7_sync_misc_ctrl	0x00	Ref7 sync miscellaneous control	R/W
0X0E0	ref8_sync_misc_ctrl	0x00	Ref8 sync miscellaneous control	R/W
0x0E1	ref9_sync_misc_ctrl	0x00	Ref9 sync miscellaneous control	R/W
0x0E2	ref10_sync_misc_ctrl	0x00	Ref10 sync miscellaneous control	R/W
0x0E3	dpll0_psl_decay_time	0x00	DPLL0 PSL decay time	R/W
0x0E4	dpll1_psl_decay_time	0x00	DPLL1 PSL decay time	R/W
0x0E5	dpll2_psl_decay_time	0x00	DPLL2 PSL decay time	R/W
0x0E6	dpll3_psl_decay_time	0x00	DPLL3 PSL decay time	R/W
0x0E7	dpll0_psl_scaling	0x00	DPLL0 PSL scaling	R/W
0x0E8	dpll1_psl_scaling	0x00	DPLL1 PSL scaling	R/W
0x0E9	dpll2_psl_scaling	0x00	DPLL2 PSL scaling	R/W
0x0EA	dpll3_psl_scaling	0x00	DPLL3 PSL scaling	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x0EC	ref_1_0_clk_sync_pair	0x10	Enables synchronization to clock and sync. (frame pulse) pair for reference inputs 0 and 1 and for each reference (0 and 1) specifies corresponding reference fed with sync pulse.	R/W
0x0ED	ref_3_2_clk_sync_pair	0x32	Enables synchronization to clock and sync. (frame pulse) pair for reference inputs 3 and 2	R/W
0x0EE	ref_5_4_clk_sync_pair	0x54	Enables synchronization to clock and sync. (frame pulse) pair for reference inputs 5 and 4	R/W
0x0EF	ref_7_6_clk_sync_pair	0x76	Enables synchronization to clock and sync. (frame pulse) pair for reference inputs 7 and 6	R/W
0x0F0	ref_9_8_clk_sync_pair	0x98	Enables synchronization to clock and sync. (frame pulse) pair for reference input 10	R/W
0x0F1	ref_10_clk_sync_pair	0x0A	Enables synchronization to clock and sync. (frame pulse) pair for reference inputs 3 and 2	R/W
0x0FF	page_sel_register	0x00	SPI Page Selection register	R/W
DPLL Configuration Registers				
0x100	dpll0_ctrl	0x0C	DPLL0 Control register	R/W
0x101	dpll0_var_bw_sel	0x00	DPLL0 Variable Bandwidth Selection register	R/W
0x102	dpll0_pull_in_hold_in	0x00	DPLL0 Pull-in Hold-in selection register	R/W
0x103	dpll0_mode_refsel	0x03	DPLL0 mode and reference selection	R/W
0x104	dpll0_refsel_stat	0x00	DPLL0 reference selection status	R
0x105	dpll0_ref_priority1_0	0x10	DPLL0 reference 1 and 0 selection priority	R/W
0x106	dpll0_ref_priority_3_2	0x32	DPLL0 reference 3 and 2 selection priority	R/W
0x107	dpll0_ref_priority_5_4	0x54	DPLL0 reference 5 and 4 selection priority	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x108	dpll0_ref_priority_7_6	0x76	DPLL0 reference 7 and 6 selection priority	R/W
0x109	dpll0_ref_priority_9_8	0x98	DPLL0 reference 9 and 8 selection priority	R/W
0x10A	dpll0_ref_priority_10	0x0A	DPLL0 reference 10 selection priority	R/W
0x10B:0x10C	dpll0_psl_max_phase	0x0000	DPLL0 PSL Maximum Phase	R/W
0x10D	dpll0_ref_fail_mask	0x87	DPLL0 reference failure mask (used for automatic reference switching and automatic holdover)	R/W
0x10E	dpll0_pfm_fail_mask	0x01	DPLL0 reference failure mask based on PFM failure indicator (used for automatic reference switching and automatic holdover)	R/W
0x10F	dpll0_ho_edge_sel	0x0B	DPLL0 Holdover Storage Delay and Reference Edge Selection register	R/W
0x110	dpll0_pbo_ctrl	0x00	Enables phase build out for DPLL0, resets the build out occurrence counter, and resets total phase build out accumulated phase	R/W
0x111	dpll0_pbo_jitter_th_ctrl	0x22	Minimum absolute phase error threshold. Below this threshold phase error is considered to be due to jitter/wander and not due to phase transient.	R/W
0x112	dpll0_pbo_mini_slope_th	0x70	Minimum phase transient slope threshold. Above this threshold phase build out will be performed.	R/W
0x113	dpll0_pbo_end_interval	0x20	Whenever this time interval is exceeded, the phase transient is considered to be finished.	R/W
0x114	dpll0_pbo_time_out	0x64	Timeout interval, after which if minimum phase slope continues to be exceeded, dpll0 will enter fast lock	R/W
0x115	dpll0_pbo_counter	0x00	Status register which indicates number of phase build out occurrences for DPLL0	R

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x116:0x118	dpll0_pbo_magnitude	0x000000	Status register which shows total cumulative phase error due to phase build out for DPLL0	R
0x119	dpll0_damping_ctrl	0x05	DPLL0 damping factor	R/W
0x120	dpll1_ctrl	0x0C	DPLL1 Control register	R/W
0x121	dpll1_var_bw_sel	0x00	DPLL1 Variable Bandwidth Selection register	R/W
0x122	dpll1_pull_in_hold_in	0x00	DPLL1 Pull-in Hold-in selection register	R/W
0x123	dpll1_mode_refsel	0x03	DPLL1 mode and reference selection	R/W
0x124	dpll1_refsel_stat	0x00	DPLL1 reference selection status	R
0x125	dpll1_ref_priority_1_0	0x10	DPLL1 reference 1 and 0 selection priority	R/W
0x126	dpll1_ref_priority_3_2	0x32	DPLL1 reference 3 and 2 selection priority	R/W
0x127	dpll1_ref_priority_5_4	0x54	DPLL1 reference 5 and 4 selection priority	R/W
0x128	dpll1_ref_priority_7_6	0x76	DPLL1 reference 7 and 6 selection priority	R/W
0x129	dpll1_ref_priority_9_8	0x98	DPLL1 reference 9 and 8 selection priority	R/W
0x12A	dpll1_ref_priority_10	0x0A	DPLL1 reference 10 selection priority	R/W
0x12B:0x12C	dpll1_psl_max_phase	0x0000	DPLL1 PSL Maximum Phase	R/W
0x12D	dpll1_ref_fail_mask	0x87	DPLL1 reference failure mask (used for automatic reference switching and automatic holdover)	R/W
0x12E	dpll1_pfm_fail_mask	0x01	DPLL1 reference failure mask based on PFM failure indicator (used for automatic reference switching and automatic holdover)	R/W
0x12F	dpll1_ho_edge_sel	0x0B	DPLL1 Holdover Storage Delay and Reference Edge Selection register	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x130	dpll1_pbo_ctrl	0x00	Enables phase build out for DPLL1, resets the build out occurrence counter, and resets total phase build out accumulated phase	R/W
0x131	dpll1_pbo_jitter_th_ctrl	0x22	Minimum absolute phase error threshold. Below this threshold phase error is considered to be due to jitter/wander and not due to phase transient.	R/W
0x132	dpll1_pbo_mini_slope_th	0x70	Minimum phase transient slope threshold. Above this threshold phase build out will be performed.	R/W
0x133	dpll1_pbo_end_interval	0x20	Whenever this time interval is exceeded, the phase transient is considered to be finished.	R/W
0x134	dpll1_pbo_time_out	0x64	Timeout interval, after which if minimum phase slope continues to be exceeded, dpll1 will enter fast lock	R/W
0x135	dpll1_pbo_counter	0x00	Status register which indicates number of phase build out occurrences for DPLL1	R
0x136:0x138	dpll1_pbo_magnitude	0x000000	Status register which shows total cumulative phase error due to phase build out for DPLL1	R
0x139	dpll1_damping_ctrl	0x05	DPLL1 damping factor	R/W
0x140	dpll2_ctrl	0x0C	DPLL2 Control register	R/W
0x141	dpll2_var_bw_sel	0x00	DPLL2 Variable Bandwidth Selection register	R/W
0x142	dpll2_pull_in_hold_in	0x00	DPLL2 Pull-in Hold-in selection register	R/W
0x143	dpll2_mode_refsel	0x03	DPLL2 mode and reference selection	R/W
0x144	dpll2_refsel_stat	0x00	DPLL2 reference selection status	R
0x145	dpll2_ref_priority_1_0	0x10	DPLL2 reference 1 and 0 selection priority	R/W
0x146	dpll2_ref_priority_3_2	0x32	DPLL2 reference 3 and 2 selection priority	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x147	dpll2_ref_priority_5_4	0x54	DPLL2 reference 5 and 4 selection priority	R/W
0x148	dpll2_ref_priority_7_6	0x76	DPLL2 reference 7 and 6 selection priority	R/W
0x149	dpll2_ref_priority_9_8	0x98	DPLL2 reference 9 and 8 selection priority	R/W
0x14A	dpll2_ref_priority_10	0x0A	DPLL2 reference 10 selection priority	R/W
0x14B:0x14C	dpll2_psl_max_phase	0x0000	DPLL2 PSL Maximum Phase	R/W
0x14D	dpll2_ref_fail_mask	0x87	DPLL2 reference failure mask (used for automatic reference switching and automatic holdover)	R/W
0x14E	dpll2_pfm_fail_mask	0x01	DPLL2 reference failure mask based on PFM failure indicator (used for automatic reference switching and automatic holdover)	R/W
0x14F	dpll2_ho_edge_sel	0x0B	DPLL2 Holdover Storage Delay and Reference Edge Selection register	R/W
0x150	dpll2_pbo_ctrl	0x00	Enables phase build out for DPLL2, resets the build out occurrence counter, and resets total phase build out accumulated phase	R/W
0x151	dpll2_pbo_jitter_th_ctrl	0x22	Minimum absolute phase error threshold. Below this threshold phase error is considered to be due to jitter/wander and not due to phase transient.	R/W
0x152	dpll2_pbo_mini_slope_th	0x70	Minimum phase transient slope threshold. Above this threshold phase build out will be performed.	R/W
0x153	dpll2_pbo_end_interval	0x20	Whenever this time interval is exceeded, the phase transient is considered to be finished.	R/W
0x154	dpll2_pbo_time_out	0x64	Timeout interval, after which if minimum phase slope continues to be exceeded, dpll2 will enter fast lock	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x155	dpll2_pbo_counter	0x00	Status register which indicates number of phase build out occurrences for DPLL2	R
0x156:0x158	dpll2_pbo_magnitude	0x000000	Status register which shows total cumulative phase error due to phase build out for DPLL2	R
0x159	dpll2_damping_ctrl	0x05	DPLL2 damping factor	R/W
0x160	dpll3_ctrl	0x0C	DPLL3 Control register	R/W
0x161	dpll3_var_bw_sel	0x00	DPLL3 Variable Bandwidth Selection register	R/W
0x162	dpll3_pull_in_hold_in	0x00	DPLL3 Pull-in Hold-in selection register	R/W
0x163	dpll3_mode_refsel	0x03	DPLL3 mode and reference selection	R/W
0x164	dpll3_refsel_stat	0x00	DPLL3 reference selection status	R
0x165	dpll3_ref_priority_1_0	0x10	DPLL3 reference 1 and 0 selection priority	R/W
0x166	dpll3_ref_priority_3_2	0x32	DPLL3 reference 3 and 2 selection priority	R/W
0x167	dpll3_ref_priority_5_4	0x54	DPLL3 reference 5 and 4 selection priority	R/W
0x168	dpll3_ref_priority_7_6	0x76	DPLL3 reference 7 and 6 selection priority	R/W
0x169	dpll3_ref_priority_9_8	0x98	DPLL3 reference 9 and 8 selection priority	R/W
0x16A	dpll3_ref_priority_10	0x0A	DPLL3 reference 10 selection priority	R/W
0x16B:0x16C	dpll3_psl_max_phase	0x0000	DPLL3 PSL Maximum Phase	R/W
0x16D	dpll3_ref_fail_mask	0x87	DPLL3 reference failure mask (used for automatic reference switching and automatic holdover)	R/W
0x16E	dpll3_pfm_fail_mask	0x01	Enables phase build out for DPLL3, resets the build out occurrence counter, and resets total phase build out accumulated phase	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x16F	dpll3_ho_edge_sel	0x0B	DPLL3 Holdover Storage Delay and Reference Edge Selection register	R/W
0x170	dpll3_pbo_ctrl	0x00	Enables phase build out for DPLL3, resets the build out occurrence counter, and resets total phase build out status	R/W
0x171	dpll3_pbo_jitter_th_ctrl	0x22	Minimum absolute phase error threshold. Below this threshold phase error is considered to be due to jitter/wander and not due to phase transient.	R/W
0x172	dpll3_pbo_mini_slope_th	0x70	Minimum phase transient slope threshold. Above this threshold phase build out will be performed.	R/W
0x173	dpll3_pbo_end_interval	0x20	Whenever this time interval is exceeded, the phase transient is considered to be finished.	R/W
0x174	dpll3_pbo_time_out	0x64	Timeout interval, after which if minimum phase slope continues to be exceeded, dpll3 will enter fast lock	R/W
0x175	dpll3_pbo_counter	0x00	Status register which indicates number of phase build out occurrences for DPLL3	R
0x176:0x178	dpll3_pbo_magnitude	0x000000	Status register which shows total cumulative phase error due to phase build out for DPLL3	R
0x179	dpll3_damping_ctrl	0x05	DPLL3 damping factor	R/W
0x17F	page_sel_register	0x00	Page Selection register	R/W
0x180	dpll_hold_lock_status	0x00	DPLL Lock and holdover status	StickyR/W
0x181	ext_fb_ctrl	0x00	External Feedback Control	R/W
0x182	dpll_config	0x04	DPLL configuration register	R/W
0x183	dpll_lock_selection	0x00	DPLL lock selection	R/W
DPLL Delta Frequency Registers				
0x18D:0x191	dpll0_df_offset	0x0000000000	DPLL0 Delta Frequency offset	W
0x192:0x196	dpll1_df_offset	0x0000000000	DPLL1 Delta Frequency offset	W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x197:0x19B	dpll2_df_offset	0x0000000000	DPLL2 Delta Frequency offset	W
0x19C:0x1A0	dpll3_df_offset	0x0000000000	DPLL3 Delta Frequency offset	W
Output Synthesizer Configuration Registers				
0x1B0	synth_drive_pll	0xE4	DPLL to Synthesizer assignment selection	R/W
0x1B1	synth_enable	0x03	Synthesizer Enable register	R/W
0x1B6	sync_fail_flag_status	0x00	Synthesizer APLL syncFailFlag status	R
0x1B7	clear_sync_fail_flag	0x00	Synthesizer APLL clear syncFail-Flag	R/W
Output Reference Selection and Output Driver Control				
0x1B8:0x1B9	synth0_base_freq	0x9C40	Synthesizer0 base frequency Bs0	R/W
0x1BA:0x1BB	synth0_freq_multiple	0x0798	Synthesizer0 base frequency multiple Ks0	R/W
0x1BC:0x1BF	synth0_ratio_M_N	0x00010001	Synthesizer0 Forward Error Correction (FEC) multiplication ratio Ms0 / Ns0 (numerator Ms0 and denominator Ns0 values)	R/W
0x1C0:0x1C1	synth1_base_freq	0x61A8	Synthesizer1 base frequency Bs1	R/W
0x1C2:0x1C3	synth1_freq_multiple	0x0C35	Synthesizer1 base frequency multiple Ks1	R/W
0x1C4:0x1C7	synth1_ratio_M_N	0x00010001	Synthesizer1Forward Error Correction (FEC) multiplication ratio Ms1 / Ns1 (numerator Ms0 and denominator Ns1 values)	R/W
0x1C8:0x1C9	synth2_base_freq	0x9C40	Synthesizer2 base frequency Bs2	R/W
0x1CA:0x1CB	synth2_freq_multiple	0x0798	Synthesizer2 base frequency multiple Ks2	R/W
0x1CC:0x1CF	synth2_ratio_M_N	0x00010001	Synthesizer2 Forward Error Correction (FEC) multiplication ratio Ms2 / Ns2 (numerator Ms0 and denominator Ns2 values)	R/W
0x1D0:0x1D1	synth3_base_freq	0x9C40	Synthesizer3 base frequency Bs3	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x1D2:0x1D3	synth3_freq_multiple	0x0798	Synthesizer3 base frequency multiple Ks3	R/W
0x1D4:0x1D7	synth3_ratio_M_N	0x00010001	Synthesizer3 Forward Error Correction (FEC) multiplication ratio Ms3 / Ns3 (numerator Ms3 and-denominator Ns3 values)	R/W
0x1FF	page_sel_register	0x00	SPI Page Selection register	R/W
0x200:0x202	synth0_post_div_A	0x000002	Synthesizer0 Post Divider A	R/W
0x203:0x205	synth0_post_div_B	0x000002	Synthesizer0 Post Divider B	R/W
0x206:0x208	synth0_post_div_C	0x000040	Synthesizer0 Post Divider C	R/W
0x209:0x20B	synth0_post_div_D	0x000040	Synthesizer0 Post Divider D	R/W
0x20C:0x20E	synth1_post_div_A	0x000002	Synthesizer1 Post Divider A	R/W
0x20F:0x211	synth1_post_div_B	0x000002	Synthesizer1 Post Divider B	R/W
0x212:0x214	synth1_post_div_C	0x000032	Synthesizer1 Post Divider C	R/W
0x215:0x217	synth1_post_div_D	0x000032	Synthesizer1 Post Divider D	R/W
0x218:0x21A	synth2_post_div_A	0x000000	Synthesizer2 Post Divider A	R/W
0x21B:0x21D	synth2_post_div_B	0x000000	Synthesizer2 Post Divider B	R/W
0x21E:0x220	synth2_post_div_C	0x000000	Synthesizer2 Post Divider C	R/W
0x221:0x223	synth2_post_div_D	0x000000	Synthesizer2 Post Divider D	R/W
0x224:0x226	synth3_post_div_A	0x000000	Synthesizer3 Post Divider A	R/W
0x227:0x229	synth3_post_div_B	0x000000	Synthesizer3 Post Divider B	R/W
0x22A:0x22C	synth3_post_div_C	0x000000	Synthesizer3 Post Divider C	R/W
0x22D:0x22F	synth3_post_div_D	0x000000	Synthesizer3 Post Divider D	R/W
0x234:0x235	phase_shift_s0_postdiv_c	0x0000	Synthesizer0 Post Divider C phase shift	R/W
0x236:0x237	phase_shift_s0_postdiv_d	0x0000	Synthesizer0 Post Divider D phase shift	R/W
0x23C:0x23D	phase_shift_s1_postdiv_c	0x0000	Synthesizer1 Post Divider C phase shift	R/W
0x23E:0x23F	phase_shift_s1_postdiv_d	0x0000	Synthesizer1 Post Divider D phase shift	R/W
0x244:0x245	phase_shift_s2_postdiv_c	0x0000	Synthesizer2 Post Divider C phase shift	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x246:0x247	phase_shift_s2_postdiv_d	0x0000	Synthesizer2 Post Divider D phase shift	R/W
0x24C:0x24D	phase_shift_s3_postdiv_c	0x0000	Synthesizer3 Post Divider C phase shift	R/W
0x24E:0x24F	phase_shift_s3_postdiv_d	0x0000	Synthesizer3 Post Divider D phase shift	R/W
0x250	synth0_fine_phase_shift	0x00	Synth0 fine phase shift (skew) in steps of VCO period over 256	R/W
0x251	synth1_fine_phase_shift	0x00	Synth1 fine phase shift (skew) in steps of VCO period over 256	R/W
0x252	synth2_fine_phase_shift	0x00	Synth2 fine phase shift (skew) in steps of VCO period over 256	R/W
0x253	synth3_fine_phase_shift	0x00	Synth3 fine phase shift (skew) in steps of VCO period over 256	R/W
0x254	synth1_0_stop_clk	0x00	Synthesizer0 and Synthesizer1 Post Dividers D and C stop clock	R/W
0x255	synth3_2_stop_clk	0x00	Synthesizer3 and Synthesizer2 Post Dividers D and C stop clock	R/W
0x261	hp_diff_en	0x00	High Performance Differential Output enable	R/W
0x262	hp_cmos_en	0x00	High Performance CMOS Output enable	R/W
GPIO Related Registers				
0x266	gpio_function_pin0	0x00	GPIO0 select or status	R/W
0x267	gpio_function_pin1	0x00	GPIO1 select or status	R/W
0x268	gpio_function_pin2	0x60	GPIO2 select or status	R/W
0x269	gpio_function_pin3	0x00	GPIO3 select or status	R/W
0x26A	gpio_function_pin4	0x00	GPIO4 select or status	R/W
0x26B	gpio_function_pin5	0x00	GPIO5 select or status	R/W
0x26C	gpio_function_pin6	0x00	GPIO6 select or status	R/W
0x276	gpio_in_6_0	0x00	GPIO6:0 Input Register	R
0x278	gpio_out_6_0	0x00	GPIO6:0 Output Register	R/W
0x27A	gpio_out_en_6_0	0x00	GPIO6:0 Output Enable Register	R/W
0x27C	gpio_latch_6_0	0x00	GPIO6:0 Latch Register	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x27F	page_sel_register	0x00	SPI Page Selection register	R/W
Addtional DPLL Control Registers				
0x2C2	dpll0_fast_lock_ctrl	0x01	DPLL0 Fast Lock Control	R/W
0x2C3	dpll0_fast_lock_phase_error_threshold	0xFF	DPLL0 Fast Lock Phase Error Threshold	R/W
0x2C4	dpll0_fast_lock_freq_errors_threshold	0x04	DPLL0 Fast Lock Frequency Error Threshold	R/W
0x2C5	dpll1_fast_lock_ctrl	0x01	DPLL1 Fast Lock Control	R/W
0x2C6	dpll1_fast_lock_phase_error_threshold	0xFF	DPLL1 Fast Lock Phase Error Threshold	R/W
0x2C7	dpll2_fast_lock_freq_errors_threshold	0x04	DPLL1 Fast Lock Frequency Error Threshold	R/W
0x2C8	dpll2_fast_lock_ctrl	0x01	DPLL2 Fast Lock Control	R/W
0x2C9	dpll2_fast_lock_phase_error_threshold	0xFF	DPLL2 Fast Lock Phase Error Threshold	R/W
0x2CA	dpll2_fast_lock_freq_errors_threshold	0x04	DPLL2 Fast Lock Frequency Error Threshold	R/W
0x2CB	dpll3_fast_lock_ctrl	0x01	DPLL3 Fast Lock Control	R/W
0x2CC	dpll3_fast_lock_phase_error_threshold	0xFF	DPLL3 Fast Lock Phase Error Threshold	R/W
0x2CD	dpll3_fast_lock_freq_errors_threshold	0x04	DPLL3 Fast Lock Frequency Error Threshold	R/W
0x2CE	dpll_fast_lock_error_status	0x00	DPLL Fast Lock Phase and Frequency Error Status	StickyR/W
0x2CF	dpll_fcl_ctl	0x00	FCL Control	R/W
0x2D4	dpll0_holdover_filt_ctrl	0x00	DPLL0 Filter Value	R/W
0x2D5	dpll1_holdover_filt_ctrl	0x00	DPLL1 Filter Value	R/W
0x2D6	dpll2_holdover_filt_ctrl	0x00	DPLL2 Filter Value	R/W
0x2D7	dpll3_holdover_filt_ctrl	0x00	DPLL3 Filter Value	R/W
0x2D8	dpll0_nco_ref_switch_ctrl	0x00	DPLL0 NCO Ref-switch Control	R/W
0x2D9	dpll1_nco_ref_switch_ctrl	0x00	DPLL1 NCO Ref-switch Control	R/W
0x2DA	dpll2_nco_ref_switch_ctrl	0x00	DPLL2 NCO Ref-switch Control	R/W
0x2DB	dpll3_nco_ref_switch_ctrl	0x00	DPLL3 NCO Ref-switch Control	R/W

Table 8 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x2DC	dpll0_lock_delay	0x00	DPLL0 Lock Time Delay	R/W
0x2DD	dpll1_lock_delay	0x00	DPLL1 Lock Time Delay	R/W
0x2DE	dpll2_lock_delay	0x00	DPLL2 Lock Time Delay	R/W
0x2DF	dpll3_lock_delay	0x00	DPLL3 Lock Time Delay	R/W
0x2E0	dpll0_fp_lock_criteria	0x00	DPLL0 Frame Pulse Lock Criteria	R/W
0x2E1	dpll1_fp_lock_criteria	0x00	DPLL1 Frame Pulse Lock Criteria	R/W
0x2E2	dpll2_fp_lock_criteria	0x00	DPLL2 Frame Pulse Lock Criteria	R/W
0x2E3	dpll3_fp_lock_criteria	0x00	DPLL3 Frame Pulse Lock Criteria	R/W
0x2E4	ref0_sync_offset_comp	0x00	Ref0 Sync Offset Compensation	R/W
0x2E5	ref1_sync_offset_comp	0x00	Ref1 Sync Offset Compensation	R/W
0x2E6	ref2_sync_offset_comp	0x00	Ref2 Sync Offset Compensation	R/W
0x2E7	ref3_sync_offset_comp	0x00	Ref3 Sync Offset Compensation	R/W
0x2E8	ref4_sync_offset_comp	0x00	Ref4 Sync Offset Compensation	R/W
0x2E9	ref5_sync_offset_comp	0x00	Ref5 Sync Offset Compensation	R/W
0x2EA	ref6_sync_offset_comp	0x00	Ref6 Sync Offset Compensation	R/W
0x2EB	ref7_sync_offset_comp	0x00	Ref7 Sync Offset Compensation	R/W
0x2EC	ref8_sync_offset_comp	0x00	Ref8 Sync Offset Compensation	R/W
0x2ED	ref9_sync_offset_comp	0x00	Ref9 Sync Offset Compensation	R/W
0x2EE	ref10_sync_offset_comp	0x00	Ref10 Sync Offset Compensation	R/W
0x2FA	dpll0_ref_sync_ctrl	0x00	DPLL0 Ref/Sync Control	R/W
0x2FB	dpll1_ref_sync_ctrl	0x00	DPLL1 Ref/Sync Control	R/W
0x2FC	dpll2_ref_sync_ctrl	0x00	DPLL2 Ref/Sync Control	R/W
0x2FD	dpll3_ref_sync_ctrl	0x00	DPLL3 Ref/Sync Control	R/W
0x2FF	page_sel_register	0x00	SPI Page Selection register	R/W

Table 8 - Register Map (continued)

8.0 Detailed Register Map

Register_Address: **0x000**
Register Name: **ready**
Default Value: **0x1F**
Type: R

Bit Field	Function Name	Description
7	Ready indication	After reset this bit goes high when device is ready. This signals that user can start to program/configure the device.
6:5	Reserved	Leave as default
4:0	Chip family identification	Family Identification = 0b11111

Register_Address: **0x001**
Register Name: **chip_id_reg**
Default Value: **0xA2**
Type: **R**

Bit Field	Function Name	Description
7:0	Chip id	Chip identification number: Unsigned binary value of these bits represent chip identification number. Customer should not write to this register.

Register_Address: **0x002**
Register Name: **hw_rev_reg**
Default Value: **0x05**
Type: **R**

Bit Field	Function Name	Description
7:0	Chip Hardware Revision register	Chip hardware revision number: Unsigned binary value of these bits represent chip hardware revision number. Customer should not write to this register.

Register_Address: **0x00B:0x00E**
Register Name: **central_freq_offset**
Default Value: **0x046AAAAB**
Type: **R/W**

Bit Field	Function Name	Description
31:0	Central frequency offset	2's complement binary value of these bits represent central frequency offset for the device. This value should be used to compensate for oscillator inaccuracy. This register the controls central frequency of all 4 Synthesizers. Expressed in steps of +/- 2^-32 of nominal setting. When the oscillator inaccuracy is known: inacc_osc = (f_osc - f_nom)/f_nom (usually specified in ppm), value to be programmed in this register is calculated using the following formula: X = (1/(1 + inacc_osc) - 1)*2^32, when f_osc < f_nom X = (1/(1 + inacc_osc))*2^32, when f_osc > f_nom, where inacc_osc - represents oscillator frequency inaccuracy, f_osc - represents oscillator frequency, and f_nom - represents oscillator nominal frequency (i.e. 25MHz, 20MHz or 50MHz) Generally, when the oscillator frequency is lower than the nominal, frequency offset has to be programmed to compensate it in opposite direction, i.e. frequency offset has to be positive, and vice versa. Example 1): if oscillator inaccuracy is -2% (f_osc = 24.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = -0.02), X= (1/(1+(-0.02)) - 1)*2^32 = (1/0.98 - 1)*2^32 = 87652394 = 0x0539782A Example 2): if oscillator inaccuracy is +2% (f_osc = 25.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = 0.02), X= (1/(1+ 0.02))*2^32 = (1/1.02)*2^32 = 4210752251 = 0xFAFAFAFB **Note 1:**With master clock frequencies of 49.152 or 24.576 MHz, the default value of this register should be maintained (0x046AAAAB). **Note 2:** Central Frequency Offset should not exceed +/-5% off nominal. **Note 3:** The **spurs_supression** register must be programmed after changing the **central_freq_offset**, even if the value has not changed.

Register_Address: **0x010**
Register Name: **spurs_supression**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	Spurs_supression	This register is used for spurs suppression. Depending on the synthesizer configuration GUI will generate recommended value. When this register is changed, the ZL30162 requires 85 msec to reconfigure itself. No reads or writes to the device are permitted during this configuration period. The **spurs_suppression** register should only be written with values recommended by the GUI. **Note:** This register must be programmed after changing the **central_freq_offset** even if the value has not changed.

Register_Address: **0x011**
Register Name: **sticky_lock**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	Sticky Lock Register	This register needs to be set to a non-zero value prior to clearing sticky (status) registers, to avoid race condition that can happen when the internal state machine updates the status register while the host clears it. Setting this register to a non-zero value stops the updating of any of the sticky registers, and clearing this register restarts the updating of the sticky registers. For proper sticky register monitoring, see the procedure under **Reading from Sticky Read (StickyR) Registers** in section 7.0, “Register Map“ on page 53.

Register_Address: **0x020**
Register Name: **ref_fail_isr_status_7_0**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7	Ref7 Fail	This bit will be set high when 'Ref7 fail mask' bit of the **ref_fail_isr_mask_7_0** register is high and conditions for Ref7 failure have occurred. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so once set it will stay high until the user clears it. Conditions for Ref7 failure are satisfied when either of LOS (external Loss of Signal), SCM (Single Cycle Monitor), CFM (Coarse Frequency Monitor), GST (Guard Soak Timer) or PFM (Precise Frequency Monitor) indicators are active and the appropriate mask bit (specified in the **ref_mon_fail_mask_X** register) is high. The failure indicators can be checked in the **ref_mon_fail_X** register.
6	Ref6 Fail	See Ref7 above
5	Ref5 Fail	See Ref7 above
4	Ref4 Fail	See Ref7 above
3	Ref3 Fail	See Ref7 above
2	Ref2 Fail	See Ref7 above
1	Ref1 Fail	See Ref7 above
0	Ref0 Fail	See Ref7 above

Register_Address: **0x021**
Register Name: **ref_fail_isr_status_10_8**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2	Ref10 Fail	See register at address 0x020 bit 7 (Ref7) for description
1	Ref9 Fail	See register at address 0x020 bit 7 (Ref7) for description
0	Ref8 Fail	See register at address 0x020 bit 7 (Ref7) for description

Register_Address: **0x022**
Register Name: **dpll_isr_status**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7	DPLL3 Lost Lock	The device will set this bit to high when 'DPLL3 Lost Lock Mask' bit of the dpll_isr_mask register is high and DPLL3 has lost lock. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** The lost lock indicator can be checked in the **dpll_hold_lock_status** register on page 163.
6	DPLL3 Holdover	The device will set this bit to high when 'DPLL3 Holdover Mask' bit of the dpll_isr_mask register is high and DPLL3 went into holdover mode. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** The lost lock indicator can be checked in the **dpll_hold_lock_status** register on page 163.
5	DPLL2 Lost Lock	The device will set this bit to high when 'DPLL2 Lost Lock Mask' bit of the dpll_isr_mask register is high and DPLL2has lost lock. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** The lost lock indicator can be checked in the **dpll_hold_lock_status** register on page 163.
4	DPLL2 Holdover	The device will set this bit to high when 'DPLL2 Holdover Mask' bit of the dpll_isr_mask register is high and DPLL2 went into holdover mode. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** The lost lock indicator can be checked in the **dpll_hold_lock_status** register on page 163.
3	DPLL1 Lost Lock	The device will set this bit to high when 'DPLL1 Lost Lock Mask' bit of the dpll_isr_mask register is high and DPLL1 has lost lock. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** The lost lock indicator can be checked in the **dpll_hold_lock_status** register on page 163.
2	DPLL1 Holdover	The device will set this bit to high when 'DPLL1 Holdover Mask' bit of the dpll_isr_mask register is high and DPLL1 went into holdover mode. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** The lost lock indicator can be checked in the **dpll_hold_lock_status** register on page 163.

Register_Address: **0x022**
Register Name: **dpll_isr_status**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
1	DPLL0 Lost Lock	The device will set this bit to high when 'DPLL0 Lost Lock Mask' bit of the dpll_isr_mask register is high and DPLL0 has lost lock. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** The lost lock indicator can be checked in the **dpll_hold_lock_status** register on page 163.
0	DPLL0 Holdover	The device will set this bit to high when 'DPLL0 Holdover Mask' bit of the dpll_isr_mask register is high and DPLL0 went into holdover mode. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** The lost lock indicator can be checked in the **dpll_hold_lock_status** register on page 163.

Register_Address: **0x023**
Register Name: **ref_fail_isr_mask_7_0**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7	Ref7 Fail Mask	When set to high, this bit allows Ref7 fail indicator to appear in the ref_fail_isr_status_7_0 register and on the IRQ line. When low, the Ref7 failure indicator is masked.
6	Ref6 Fail Mask	See description for Ref7 above
5	Ref5 Fail Mask	See description for Ref7 above
4	Ref4 Fail Mask	See description for Ref7 above
3	Ref3 Fail Mask	See description for Ref7 above
2	Ref2 Fail Mask	See description for Ref7 above
1	Ref1 Fail Mask	See description for Ref7 above
0	Ref0 Fail Mask	See description for Ref7 above

Register_Address: **0x024**
Register Name: **ref_fail_isr_mask_10_8**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2	Ref10 Fail Mask	See description for register at address 0x023, bit 7 (Ref 7)
1	Ref9 Fail Mask	See description for register at address 0x023, bit 7 (Ref 7)
0	Ref8 Fail Mask	See description for register at address 0x023, bit 7 (Ref 7)

Register_Address: **0x025**
Register Name: **dpll_isr_mask**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7	DPLL3 Lost Lock Mask	When set to high, this bit allows DPLL3 lost lock indicator to appear in the dpll_isr_status register and on the IRQ line. When low, the DPLL3 lost lock indicator is masked.
6	DPLL3 Holdover Mask	When set to high, this bit allows DPLL3 holdover indicator to appear in the dpll_isr_status register and on the IRQ line. When low, the DPLL3 holdover indicator is masked.
5	DPLL2 Lost Lock	When set to high, this bit allows DPLL2 lost lock indicator to appear in the dpll_isr_status register and on the IRQ line. When low, the DPLL2 lost lock indicator is masked.
4	DPLL2 Holdover	When set to high, this bit allows DPLL2 holdover indicator to appear in the dpll_isr_status register and on the IRQ line. When low, the DPLL2 holdover indicator is masked.
3	DPLL1 Lost Lock	When set to high, this bit allows DPLL1 lost lock indicator to appear in the dpll_isr_status register and on the IRQ line. When low, the DPLL1 lost lock indicator is masked.
2	DPLL1 Holdover	When set to high, this bit allows DPLL1 holdover indicator to appear in the dpll_isr_status register and on the IRQ line. When low, the DPLL1 holdover indicator is masked.
1	DPLL0 Lost Lock	When set to high, this bit allows DPLL0 lost lock indicator to appear in the dpll_isr_status register and on the IRQ line. When low, the DPLL0 lost lock indicator is masked.

Register_Address: **0x025**
Register Name: **dpll_isr_mask**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
0	DPLL0 Holdover	When set to high, this bit allows DPLL0 holdover indicator to appear in the dpll_isr_status register and on the IRQ line. When low, the DPLL0 holdover indicator is masked.

Register_Address: **0x026**
Register Name: **ref_mon_fail_0**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref0 Fail PFM	Ref0 Precise Frequency Monitor (PFM) failure: This bit is set high when Ref0 fails to meet the Precise Frequency Monitor (PFM) failure criteria specified by the 'PFM limit' bits of the pfm_limit_ref1_0 register. The PFM failure criteria is typically referred to as reference frequency drift. This bit is 'sticky', so it will remain high until the user clears it. **Note:** This bit is not maskable, i.e. whenever conditions for it to be set are met, it will be set, regardless of any mask bits
3	Ref0 Fail GST	Guard Soak Timer failure (GST): This bit is set when Ref0 fails to meet Guard Soak Timer (GST) failure criteria specified by the 'GST disqualify Ref0' bits of the gst_disqualif_time_3_0 register. The GST timer is triggered by either CFM or SCM failure and this bit will be set if either of the two failures still exists upon expiration of the GST time. This bit is 'sticky', so it will stay high until customer clears it. **Note:** This bit is not maskable, i.e. whenever conditions for it to be set are met, it will be set, regardless of any mask bits
2	Ref0 Fail CFM	Ref0 Coarse Frequency Monitor (CFM) failure: This bit is set this when Ref0 fails to meet Coarse Frequency Monitor (CFM) failure criteria specified by the 'Ref0 CFM Limit' bits of the scm_cfm_limit_ref0 register. The CFM failure criteria is usually referred to as reference phase hit. This bit is 'sticky', so it will stay high until customer clears it. **Note:** this bit is not maskable, i.e. whenever conditions for it to be set are met, it will be set, regardless of any mask bits
1	Ref0 Fail SCM	Ref0 Single Cycle Monitor (SCM) failure: This bit is set when Ref0 fails to meet Single Cycle Monitor (SCM) failure criteria specified by the 'Ref0 SCM limit' bits of the scm_cfm_limit_ref0 register. The SCM failure criteria is usually referred to as reference phase irregularity. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever conditions for it to be set are met, it will be set, regardless of any mask bits

Register_Address: **0x026**
Register Name: **ref_mon_fail_0**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
0	Ref0 Fail LOS	External Ref0 Loss Of Signal (LOS) indicator: This bit is set when the external Ref0 LOS signal, applied to a selected GPIO, goes high. This bit is 'sticky', so it will stay high until the user clears it. The Ref0 LOS signal can be selected to appear on any of available GPIOs through the gpio_function_pin[0:6] registers. **Note:** this bit is not maskable, i.e. whenever conditions for it to be set are met, it will be set, regardless of any mask bits

Register_Address: **0x027**
Register Name: **ref_mon_fail_1**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref1 Fail PFM	Ref1 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref1 Fail GST	Ref1 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref1 Fail CFM	Ref1 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref1 Fail SCM	Ref1 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref1 Fail LOS	Ref1 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x028**
Register Name: **ref_mon_fail_2**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref2 Fail PFM	Ref2 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref2 Fail GST	Ref2 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3

Register_Address: **0x028**
Register Name: **ref_mon_fail_2**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
2	Ref2 Fail CFM	Ref2 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref2 Fail SCM	Ref2 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref2 Fail LOS	Ref2 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x029**
Register Name: **ref_mon_fail_3**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref3 Fail PFM	Ref3 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref3 Fail GST	Ref3 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref3 Fail CFM	Ref3 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref3 Fail SCM	Ref3 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref3 Fail LOS	Ref3 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x02A**
Register Name: **ref_mon_fail_4**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref4 Fail PFM	Ref4 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref4 Fail GST	Ref4 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3

Register_Address: **0x02A**
Register Name: **ref_mon_fail_4**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
2	Ref4 Fail CFM	Ref4 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref4 Fail SCM	Ref4 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref4 Fail LOS	Ref4 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x02B**
Register Name: **ref_mon_fail_5**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref5 Fail PFM	Ref5 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref5 Fail GST	Ref5 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref5 Fail CFM	Ref5 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref5 Fail SCM	Ref5 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref5 Fail LOS	Ref5 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x02C**
Register Name: **ref_mon_fail_6**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref6 Fail PFM	Ref6 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4

Register_Address: **0x02C**
Register Name: **ref_mon_fail_6**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
3	Ref6 Fail GST	Ref6 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref6 Fail CFM	Ref6 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref6 Fail SCM	Ref6 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref6 Fail LOS	Ref6 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x02D**
Register Name: **ref_mon_fail_7**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref7 Fail PFM	Ref7 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref7 Fail GST	Ref7 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref7 Fail CFM	Ref7 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref7 Fail SCM	Ref7 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref7 Fail LOS	Ref7 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x02E**
Register Name: **ref_mon_fail_8**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default

Register_Address: **0x02E**
Register Name: **ref_mon_fail_8**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
4	Ref8 Fail PFM	Ref8 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref8 Fail GST	Ref8 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref8 Fail CFM	Ref8 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref8 Fail SCM	Ref8 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref8 Fail LOS	Ref8 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x02F**
Register Name: **ref_mon_fail_9**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref9 Fail PFM	Ref9 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref9 Fail GST	Ref9 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref9 Fail CFM	Ref9 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref9 Fail SCM	Ref9 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref9 Fail LOS	Ref9 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x030**
Register Name: **ref_mon_fail_10**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref10 Fail PFM	Ref10 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref10 Fail GST	Ref10 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref10 Fail CFM	Ref10 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref10 Fail SCM	Ref10 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref10 Fail LOS	Ref10 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x036**
Register Name: **ref_mon_fail_mask_0**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref0 Fail PFM Mask	When set to high, this bit will allow Ref0 Fail PFM to appear in ref_fail_isr_status_7_0 register and on IRQ line if not masked by 'Ref0 Fail Mask' bit in the ref_fail_isr_mask_7_0 register. When low, Ref0 Fail PFM will be masked from appearing in the ref_fail_isr_status_7_0 register and on IRQ line. **Note:** This bit will not affect 'Ref0 Fail PFM' bit in the ref_mon_fail_0 register since the ref_mon_fail_0 register values are not maskable.
3	Ref0 Fail GST Mask	When set to high, this bit will allow Ref0 Fail GST to appear in ref_fail_isr_status_7_0 register and on IRQ line if not masked by 'Ref0 Fail Mask' bit in the ref_fail_isr_mask_7_0 register. When low, Ref0 Fail GST will be masked from appearing in the ef_fail_isr_status_7_0 register and on IRQ line. **Note:** This bit will not affect 'Ref0 Fail GST' bit in the ref_mon_fail_0 register since the ref_mon_fail_0 register values are not maskable.

Register_Address: **0x036**
Register Name: **ref_mon_fail_mask_0**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
2	Ref0 Fail CFM Mask	When set to high, this bit will allow Ref0 Fail CFM to appear in ref_fail_isr_status_7_0 register and on IRQ line if not masked by 'Ref0 Fail Mask' bit in the ref_fail_isr_mask_7_0 register. When low, Ref0 CFM failure will be masked from appearing, as part of Ref0 failure indicator, in the ref_fail_isr_mask_7_0 register and on IRQ line. **Note:** This bit will not affect 'Ref0 Fail CFM' bit in the ref_mon_fail_0 register since the ref_mon_fail_0 register values are not maskable.
1	Ref0 Fail SCM Mask	When set to high, this bit will allow Ref0 Fail SCM to appear in ref_fail_isr_status_7_0 register and on IRQ line if not masked by 'Ref0 Fail Mask' bit in the ref_fail_isr_mask_7_0 register. When low, Ref0 SCM failure will be masked from appearing, as part of Ref0 failure indicator, in the 'Reference status interrupt failure' register and on IRQ line. **Note:** This bit will not affect 'Ref0 Fail SCM' bit in the ref_mon_fail_0 register since the ref_mon_fail_0 register values are not maskable.
0	Ref0 Fail LOS Mask	When set to high, this bit will allow Ref0 Fail LOS to appear in ref_fail_isr_status_7_0 register and on IRQ line if not masked by 'Ref0 Fail Mask' bit in the ref_fail_isr_mask_7_0 register. When low, Ref0 external LOS failure will be masked from appearing, as part of Ref0 failure indicator, in the 'Reference status interrupt failure' register and on IRQ line. **Note:** This bit will not affect 'Ref0 Fail LOS' bit in the ref_mon_fail_0 register since the ref_mon_fail_0 register values are not maskable.

Register_Address: **0x037**
Register Name: **ref_mon_fail_mask_1**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref1 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref1 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref1 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref1 Fail SCM Mask	See description for register at address 0x036 bit 1

Register_Address: **0x037**
Register Name: **ref_mon_fail_mask_1**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
0	Ref1 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x038**
Register Name: **ref_mon_fail_mask_2**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref2 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref2 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref2 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref2 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref2 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x039**
Register Name: **ref_mon_fail_mask_3**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref3 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref3 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref3 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref3 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref3 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x03A**
Register Name: **ref_mon_fail_mask_4**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref4 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref4 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref4 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref4 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref4 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x03B**
Register Name: **ref_mon_fail_mask_5**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref5 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref5 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref5 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref5 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref5 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x03C**
Register Name: **ref_mon_fail_mask_6**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref6 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref6 Fail GST Mask	See description for register at address 0x036 bit 3

Register_Address: **0x03C**
Register Name: **ref_mon_fail_mask_6**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
2	Ref6 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref6 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref6 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x03D**
Register Name: **ref_mon_fail_mask_7**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref7 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref7 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref7 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref7 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref7 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x03E**
Register Name: **ref_mon_fail_mask_8**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref8 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref8 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref8 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref8 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref8 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x03F**
Register Name: **ref_mon_fail_mask_9**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref9 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref9 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref9 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref9 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref9 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x040**
Register Name: **ref_mon_fail_mask_10**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref10 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref10 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref10 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref10 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref10 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x046**
Register Name: **gst_disqualif_time_3_0**
Default Value: **0xAA**
Type: **R/W**

Bit Field	Function Name	Description
7:6	Ref3 GST disqualification time	Guard soak timer disqualify time: Time to disqualify Ref3 input clock after detection of either a Ref3 CFM or Ref3 SCM failure indications. The expiration of the GST disqualify time after starting of the Ref3 GST disqualify timer will cause the Ref3 GST indicator to go high if the source of the timer triggering is still present. Selection: 00 = minimum delay possible 01 = 10 ms 10 = 50 ms (default) 11 = 2.5 s
5:4	Ref2 GST disqualification time	See bits 7:6 (Ref3) for details
3:2	Ref1 GST disqualification time	See bits 7:6 (Ref3) for details
1:0	Ref0 GST disqualification time	See bits 7:6 (Ref3) for details

Register_Address: **0x047**
Register Name: **gst_disqualif_time_7_4**
Default Value: **0xAA**
Type: **R/W**

Bit Field	Function Name	Description
7:6	Ref7 GST disqualification time	See description for register at address 0x046 bits 7:6
5:4	Ref6 GST disqualification time	See description for register at address 0x046 bits 7:6
3:2	Ref5 GST disqualification time	See description for register at address 0x046 bits 7:6
1:0	Ref4 GST disqualification time	See description for register at address 0x046 bits 7:6

Register_Address: **0x048**
Register Name: **gst_disqualif_time_10_8**
Default Value: **0x2A**
Type: **R/W**

Bit Field	Function Name	Description
7:6	Reserved	Leave as default
5:4	Ref10 GST disqualification time	See description for register at address 0x046 bits 7:6
3:2	Ref9 GST disqualification time	See description for register at address 0x046 bits 7:6
1:0	Ref8 GST disqualification time	See description for register at address 0x046 bits 7:6

Register_Address: **0x04A**
Register Name: **gst_qualif_time_3_0**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7:6	Ref3 GST qualification time	Guard soak timer qualify time selection: Time to qualify Ref3 input clock after disappearance of both the Ref3 CFM and the Ref3 SCM failure indications. The expiration of the GST qualify time after starting of the Ref3 GST qualify timer will cause Ref3 GST failure indicator to go low if neither the Ref3 CFM nor the Ref3 SCM indicator is present. Selection: 00 = 2 x selected Ref3 GST disqualify time 01 = 4 x selected Ref3 GST disqualify time (default) 10 = 8 x selected Ref3 GST disqualify time 11 = 16 x selected Ref3 GST disqualify time
5:4	Ref2 GST qualification time	See bits 7:6 (Ref3) for details
3:2	Ref1 GST qualification time	See bits 7:6 (Ref3) for details
1:0	Ref0 GST qualification time	See bits 7:6 (Ref3) for details

Register_Address: **0x04B**
Register Name: **gst_qualif_time_7_4**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7:6	Ref7 GST qualification time	See description for register at address 0x04A bits 7:6
5:4	Ref6 GST qualification time	See description for register at address 0x04A bits 7:6
3:2	Ref5 GST qualification time	See description for register at address 0x04A bits 7:6
1:0	Ref4 GST qualification time	See description for register at address 0x04A bits 7:6

Register_Address: **0x04C**
Register Name: **gst_qualif_time_10_8**
Default Value: **0x15**
Type: R/W

Bit Field	Function Name	Description
7:6	Reserved	Leave as default
5:4	Ref10 GST qualification time	See description for register at address 0x04A bits 7:6
3:2	Ref9 GST qualification time	See description for register at address 0x04A bits 7:6
1:0	Ref8 GST qualification time	See description for register at address 0x04A bits 7:6

Register_Address: **0x050**
Register Name: **scm_cfm_limit_ref0**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref0 SCM limit	These bits represent Ref0 Single Cycle Monitor (SCM) limit selection. When Ref0 fails the criteria specified by these bits, the SCM failure indicator will go high (can be read in the ref_mon_fail_0 register) Selection: 000 = +/- 0.1% (in Ref0 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% Note that Ref0 clock is sampled by a 800 MHz clock, so the measurement granularity is 1.25 ns. This imposes a limitation to SCM limits that can be programmed depending on Ref0 clock frequencies: +/- 0.1% can be programmed for frequencies below 800 kHz +/- 0.5%: below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz **Note 1:** The CFM and SCM limits should be set to the same value for proper operation for frequencies below 16 kHz. **Note 2:** The SCM indicator should not be used (it should be masked) for reference frequencies above 400MHz.
3	Reserved	Leave as default

Register_Address: **0x050**
Register Name: **scm_cfm_limit_ref0**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
2:0	Ref0 CFM Limit	These bits represent the Ref0 Coarse Frequency Monitor (CFM) limit selection. When Ref0 fails the criteria specified by these bits, the CFM failure indicator will go high (can be read in the ref_mon_fail_0 register). Selection: 000 = +/- 0.1% (in Ref0 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% **Note :** The CFM and SCM limits should be set to the same value for proper operation for frequencies below 16 kHz.

Register_Address: **0x051**
Register Name: **scm_cfm_limit_ref1**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref1 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref1 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x052**
Register Name: **scm_cfm_limit_ref2**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref2 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref2 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x053**
Register Name: **scm_cfm_limit_ref3**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref3 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref3 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x054**
Register Name: **scm_cfm_limit_ref4**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref4 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref4 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x055**
Register Name: **scm_cfm_limit_ref5**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref5 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref5 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x056**
Register Name: **scm_cfm_limit_ref6**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref6 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref6 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x057**
Register Name: **scm_cfm_limit_ref7**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref7 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref7 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x058**
Register Name: **scm_cfm_limit_ref8**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref8 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref8 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x059**
Register Name: **scm_cfm_limit_ref9**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref9 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref9 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x05A**
Register Name: **scm_cfm_limit_ref10**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref10 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref10 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x060**
Register Name: **pfm_limit_ref1_0**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref1 PFM Limit	These bits represent the Ref1 Precise Frequency Monitor (PFM) limit selection. When Ref1 fails this criteria, the PFM failure indicator will go high that can be read in the ref_mon_fail_1 register. Selection: 000 = 9.2 --- 12 ppm (in Ref1 frequency units) 001 = 40 --- 52 ppm 010 = 64 --- 83 ppm 011 = 100 --- 130 ppm 100 = 13.8 --- 18 ppm 101 = 24.6 --- 32 ppm 110 = 36.6 --- 47.5 ppm 111 = 52 --- 67.5 ppm **Example:** For Ref1 PFM Limit = 000, the input reference will be accepted if its frequency accuracy is lower than +/- 9.2 ppm. If the input reference frequency accuracy exceeds +/- 12 ppm, than the reference will be rejected. If the input reference frequency accuracy is in between +/-9.2 ppm and +/-12 ppm the state remains unchanged (hysteresis). **Note :** PFM supports any reference (input) frequency from 1 Hz to 750 MHz except for non integer (in Hz) frequencies below 5,000,000 Hz. For example 1 Hz, 8 kHz, 2.048 MHz, 156.25*66/64 MHz are supported frequencies but 0.5 Hz and 1.5 Hz are not supported.

Register_Address: **0x060**
Register Name: **pfm_limit_ref1_0**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
3	Reserved	Leave as default
2:0	Ref0 PFM Limit	See bits 6:4 (Ref1)

Register_Address: **0x061**
Register Name: **pfm_limit_ref3_2**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref3 PFM Limit	See description for register at address 0x060 bits 6:4
3	Reserved	Leave as default
2:0	Ref2 PFM Limit	See description for register at address 0x060 bits 2:0

Register_Address: **0x062**
Register Name: **pfm_limit_ref5_4**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref5 PFM Limit	See description for register at address 0x060 bits 6:4
3	Reserved	Leave as default
2:0	Ref4 PFM Limit	See description for register at address 0x060 bits 2:0

Register_Address: **0x063**
Register Name: **pfm_limit_ref7_6**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref7 PFM Limit	See description for register at address 0x060 bits 6:4
3	Reserved	Leave as default
2:0	Ref6 PFM Limit	See description for register at address 0x060 bits 2:0

Register_Address: **0x064**
Register Name: **pfm_limit_ref9_8**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref9 PFM Limit	See description for register at address 0x060 bits 6:4
3	Reserved	Leave as default
2:0	Ref8 PFM Limit	See description for register at address 0x060 bits 2:0

Register_Address: **0x065**
Register Name: **pfm_limit_ref10**
Default Value: **0x03**
Type: **R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2:0	Ref10 PFM Limit	See description for register at address 0x060 bits 2:0

Register_Address: **0x068**
Register Name: **phase_acq_en_7_0**
Default Value: **0xFF**
Type: **R/W**

Bit Field	Function Name	Description
7	Phase Acquisition 7 enable	When this bit is set to high, it will enable Phase Acquisition module for Ref7 input. When low, Phase Acquisition 7 is disabled (i.e. powered down).
6	Phase Acquisition 6 enable	See bit 7 for details
5	Phase Acquisition 5 enable	See bit 7 for details
4	Phase Acquisition 4 enable	See bit 7 for details
3	Phase Acquisition 3 enable	See bit 7 for details
2	Phase Acquisition 2 enable	See bit 7 for details
1	Phase Acquisition 1 enable	See bit 7 for details
0	Phase Acquisition 0 enable	See bit 7 for details

Register_Address: **0x069**
Register Name: **phase_acq_en_10_8**
Default Value: **0x07**
Type: **R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2	Phase Acquisition 10 enable	See description for register at address 0x068 bit 7
1	Phase Acquisition 9 enable	See description for register at address 0x068 bit 7
0	Phase Acquisition 8 enable	See description for register at address 0x068 bit 7

Register_Address: **0x06A**
Register Name: **phasemem_limit_ref0**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref0	These bits specify the Ref0 phase memory limit as per the following formula, using E32 series style: Value = round(32 * log(PhaseMemLimit/10)), where PhaseMemLimit is given in us units Example, if the desired phase memory limit is 10us, the value to be written to this register is 0x00, for 1 ms the value is 0x40, while for 930 seconds the value is 0xFF. **Note:** This register should be programmed to have a value that represents at least one reference period.

Register_Address: **0x06B**
Register Name: **phasemem_limit_ref1**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref1	See description for register at address 0x06A

Register_Address: **0x06C**
Register Name: **phasemem_limit_ref2**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref2	See description for register at address 0x06A

Register_Address: **0x06D**
Register Name: **phasemem_limit_ref3**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref3	See description for register at address 0x06A

Register_Address: **0x06E**
Register Name: **phasemem_limit_ref4**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref4	See description for register at address 0x06A

Register_Address: **0x06F**
Register Name: **phasemem_limit_ref5**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref5	See description for register at address 0x06A

Register_Address: **0x070**
Register Name: **phasemem_limit_ref6**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref6	See description for register at address 0x06A

Register_Address: **0x071**
Register Name: **phasemem_limit_ref7**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref7	See description for register at address 0x06A

Register_Address: **0x072**
Register Name: **phasemem_limit_ref8**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref8	See description for register at address 0x06A

Register_Address: **0x073**
Register Name: **phasemem_limit_ref9**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref9	See description for register at address 0x06A

Register_Address: **0x074**
Register Name: **phasemem_limit_ref10**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref10	See description for register at address 0x06A

Register_Address: **0x07A**
Register Name: **ref_config_7_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	Ref7 differential input enable	When this bit is set high, the device expects differential signal on its Ref7 pins (REF7_P and REF7_N). When low, the device expects single-ended signal on the REF7_P input, and the REF7_N input should be tied to GND.
6	Ref6 differential input enable	See bit 7 for details
5	Ref5 differential input enable	See bit 7 for details
4	Ref4 differential input enable	See bit 7 for details
3	Ref3 differential input enable	See bit 7 for details
2	Ref2 differential input enable	See bit 7 for details
1	Ref1 differential input enable	See bit 7 for details
0	Ref0 differential input enable	See bit 7 for details

Register_Address: **0x07B**
Register Name: **ref_config_8**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref8 differential input enable	See description for register at address 0x07A bit 7

Register_Address: **0x07C**
Register Name: **ref_pre_divide_7_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	Ref7 pre-divider enable	When this bit is set to high, the Ref7 input clock will be divided by 2 prior being processed by the DPLLs. All registers requiring Ref7 frequency information are programmed as if the divider output frequency is actual Ref7 frequency. When low, the Ref7 input clock is not divided prior being processed by the DPLLs.
6	Ref6 pre-divider enable	See bit 7 for details
5	Ref5 pre-divider enable	See bit 7 for details
4	Ref4 pre-divider enable	See bit 7 for details
3	Ref3 pre-divider enable	See bit 7 for details
2	Ref2 pre-divider enable	See bit 7 for details
1	Ref1 pre-divider enable	See bit 7 for details
0	Ref0 pre-divider enable	See bit 7 for details

Register_Address: **0x07D**
Register Name: **ref_pre_divide_10_8**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2	Ref10 pre-divider enable	See description for register at address 0x07C bit 7
1	Ref9 pre-divider enable	See description for register at address 0x07C bit 7
0	Ref8 pre-divider enable	See description for register at address 0x07C bit 7

Register_Address: **0x07F**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Page selection register	The unsigned binary value written to this register selects the 128 byte page of registers that the host can write to. 0x00: page 0 (register addresses 0x00 to 0x7F) 0x01: page 1 (register addresses 0x80 to 0xFF) 0x02: page 2 (register addresses 0x100 to 0x17F) 0x03: page 3 (register addresses 0x180 to 0x1FF) 0x04: page 4 (register addresses 0x200 to 0x27F) 0x05: page 5 (register addresses 0x280 to 0x2FF) 0x06-0xFF: reserved

Register_Address: **0x080:0x081**
Register Name: **ref0_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref0 base frequency Br0	Unsigned binary value of these bits represents Ref0 base frequency Br in Hz. Examples of values fro Br that can be programmed: 0x0001 for 1Hz, 0x000A for 10Hz, 0x0064 for 100Hz 0x03E8 for 1kHz, 0x07D0 for 2kHz, 0x1F40 for 8kHz, 0x61A8 for 25kHz, 0x9C40 for 40kHz. **Note 1:** Br has to be directly divisible from 1600000000, i.e. mod (1600000000, Br) has to be 0. The evaluation board GUI can generate recommended Br, Kr, Mr and Nr values for required input frequency. **Note 2:** in order to write e.g. 0x9C40 to this register (and any other register whose value is larger than 8 bits), 0x9C has to be written to the lower address and 0x40 to the upper address (big endian) with the 0x40 (LSBs) written last.

Register_Address: **0x082:0x083**
Register Name: **ref0_freq_multiple**
Default Value: **0x0F30**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref0 base frequency multiple Kr0	Unsigned binary value represents the Ref0 base frequency multiplication number. For a regular (non-FEC) reference frequency, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr has to equal the reference frequency in Hz. Examples of some references frequencies and appropriate values that can be programmed for Br and Kr to match that reference frequency: Ref0 frequency — Base frequency Br — Base frequency multiple Kr 2.048 MHz — 8 kHz (0x1F40) — 256 (0x0100) 1.544 MHz — 8 kHz (0x1F40) — 193 (0x00C1) 19.44 MHz — 40 kHz (0x9C40) — 486 (0x01E6) 177.5.MHz — 25 kHz (0x61A8) — 7100 (0x1BBC) 125 MHz — 40 kHz (0x9C40) — 18752 (0x4940) 156.25.MHz — 25 kHz (0x61A8) — 6250 (0x186A) 155.52 MHz — 40 kHz (0x9C40) — 3888 (0x0F30) 1234 Hz — 1 Hz (0x0001) — 1234 (0x04D2) 8 kHz — 1 kHz (0x03E8) — 8 (0x0008)

Register_Address: **0x084:0x087**
Register Name: **ref0_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref0 FEC ratio numerator Mr0	The unsigned binary value Mr, in combination with the unsigned binary value Nr represents the Ref0 FEC multiplication ratio. For FEC reference frequencies, the 'Base frequency' number, Br multiplied by the 'Base frequency multiple' number Kr, multiplied by Mr and divided by Nr has to equal the reference frequency in Hz; Ref_freq [Hz] = Br x Kr x Mr / Nr For regular (non-FEC) reference frequencies, Mr and Nr should both be programmed to 0x0001 (default values) Examples of some FEC references frequencies and appropriate values that can be programmed for the Br, Kr, Mr and Nr registers to match required FEC reference frequency: a) OC-192 mode, standard EFEC for long reach: (155.52 MHz * 255/237)
15:0	Ref0 FEC ratio denominator Nr0	Reference frequency - 155.52 MHz Base frequency Br - 40 kHz (0x9C40) Base frequency multiple Kr - 3888 (0x0F30) FEC ratio Numerator Mr - 237 (0x00ED) FEC ratio denominator Nr - 255 (0x00FF) 3888 x 255 / 237 x 40 kHz b) Long reach 10GE mode, double rate conversion (156.25 MHz x 66/64 x 255/238) : Reference frequency - 155.52 MHz Base frequency Br - 25 kHz (0x61A8) Base frequency multiple Kr - 6250 (0x186A) FEC ratio Numerator Mr - 66x255 (0x41BE) FEC ratio denominator Nr - 64x238 (0x3B80) 25 kHz x 6250 x 66/64 x 255/238

Register_Address: **0x088:0x089**
Register Name: **ref1_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref1 base frequency Br1	See description for registers at address 0x080:0x081

Register_Address: **0x08A:0x08B**
Register Name: **ref1_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref1 base frequency multiple Kr1	See description for registers at address 0x082:0x083

Register_Address: **0x08C:0x08F**
Register Name: **ref1_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref1 FEC ratio numerator Mr1	See description for registers at address 0x084:0x087
15:0	Ref1 FEC ratio denominator Nr1	

Register_Address: **0x090:0x091**
Register Name: **ref2_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref2 base frequency Br2	See description for registers at address 0x080:0x081

Register_Address: **0x092:0x093**
Register Name: **ref2_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref2 base frequency multiple Kr2	See description for registers at address 0x082:0x083

Register_Address: **0x094:0x097**
Register Name: **ref2_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref2 FEC ratio numerator Mr2	See description for registers at address 0x084:0x087
15:0	Ref2 FEC ratio denominator Nr2	

Register_Address: **0x098:0x099**
Register Name: **ref3_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref3 base frequency Br3	See description for registers at address 0x080:0x081

Register_Address: **0x09A:0x09B**
Register Name: **ref3_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref3 base frequency multiple Kr3	See description for registers at address 0x082:0x083

Register_Address: **0x09C:0x09F**
Register Name: **ref3_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref3 FEC ratio numerator Mr3	See description for registers at address 0x084:0x087
15:0	Ref3 FEC ratio denominator Nr3	

Register_Address: **0x0A0:0x0A1**
Register Name: **ref4_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref4 base frequency Br4	See description for registers at address 0x080:0x081

Register_Address: **0x0A2:0x0A3**
Register Name: **ref4_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref4 base frequency multiple Kr4	See description for registers at address 0x082:0x083

Register_Address: **0x0A4:0x0A7**
Register Name: **ref4_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref4 FEC ratio numerator Mr4	See description for registers at address 0x084:0x087
15:0	Ref4 FEC ratio denominator Nr4	

Register_Address: **0x0A8:0x0A9**
Register Name: **ref5_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref5 base frequency Br5	See description for registers at address 0x080:0x081

Register_Address: **0x0AA:0x0AB**
Register Name: **ref5_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref5 base frequency multiple Kr5	See description for registers at address 0x082:0x083

Register_Address: **0x0AC:0x0AF**
Register Name: **ref5_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref5 FEC ratio numerator Mr5	See description for registers at address 0x084:0x087
15:0	Ref5 FEC ratio denominator Nr5	

Register_Address: **0x0B0:0x0B1**
Register Name: **ref6_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref6 base frequency Br6	See description for registers at address 0x080:0x081

Register_Address: **0x0B2:0x0B3**
Register Name: **ref6_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref6 base frequency multiple Kr6	See description for registers at address 0x082:0x083

Register_Address: **0x0B4:0x0B7**
Register Name: **ref6_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref6 FEC ratio numerator Mr6	See description for registers at address 0x084:0x087
15:0	Ref6 FEC ratio denominator Nr6	

Register_Address: **0x0B8:0x0B9**
Register Name: **ref7_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref7 base frequency Br7	See description for registers at address 0x080:0x081.

Register_Address: **0x0BA:0x0BB**
Register Name: **ref7_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref7 base frequency multiple Kr7	See description for registers at address 0x082:0x083

Register_Address: **0x0BC:0x0BF**
Register Name: **ref7_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref7 FEC ratio numerator Mr7	See description for registers at address 0x084:0x087
15:0	Ref7 FEC ratio denominator Nr7	

Register_Address: **0x0C0:0x0C1**
Register Name: **ref8_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref8 base frequency Br8	See description for registers at address 0x080:0x081

Register_Address: **0x0C2:0x0C3**
Register Name: **ref8_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref8 base frequency multiple Kr8	See description for registers at address 0x082:0x083

Register_Address: **0x0C4:0x0C7**
Register Name: **ref8_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref8 FEC ratio numerator Mr8	See description for registers at address 0x084:0x087
15:0	Ref8 FEC ratio denominator Nr8	

Register_Address: **0x0C8:0x0C9**
Register Name: **ref9_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref9 base frequency Br9	See description for registers at address 0x080:0x081

Register_Address: **0x0CA:0x0CB**
Register Name: **ref9_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref9 base frequency multiple Kr9	See description for registers at address 0x082:0x083

Register_Address: **0x0CC:0x0CF**
Register Name: **ref9_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Re9 FEC ratio numerator Mr9	See description for registers at address 0x084:0x087
15:0	Ref9 FEC ratio denominator Nr9	

Register_Address: **0x0D0:0x0D1**
Register Name: **ref10_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref10 base frequency Br10	See description for registers at address 0x080:0x081

Register_Address: **0x0D2:0x0D3**
Register Name: **ref10_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref10 base frequency multiple Kr10	See description for registers at address 0x082:0x083

Register_Address: **0x0D4:0x0D7**
Register Name: **ref10_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref10 FEC ratio numerator Mr10	See description for registers at address 0x084:0x087
15:0	Ref10 FEC ratio denominator Nr10	

Register_Address: **0x0D8**
Register Name: **ref0_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref0 Frame Sync Edge Control	This bit controls expected edge alignment of the input reference sync and its associated input reference clock. Selection: 0 : Reference (as input sync) is aligned to the rising edge of the associated input reference clock 1 : Reference (as input sync) is aligned to the falling edge of the associated input reference clock

Register_Address: **0x0D9**
Register Name: **ref1_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref1 Frame Sync Edge Control	See description for registers at address 0x0D8

Register_Address: **0x0DA**
Register Name: **ref2_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref2 Frame Sync Edge Control	See description for registers at address 0x0D8

Register_Address: **0x0DB**
Register Name: **ref3_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref3 Frame Sync Edge Control	See description for registers at address 0x0D8

Register_Address: **0x0DC**
Register Name: **ref4_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref4 Frame Sync Edge Control	See description for registers at address 0x0D8

Register_Address: **0x0DD**
Register Name: **ref5_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref5 Frame Sync Edge Control	See description for registers at address 0x0D8

Register_Address: **0x0DE**
Register Name: **ref6_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref6 Frame Sync Edge Control	See description for registers at address 0x0D8

Register_Address: **0x0DF**
Register Name: **ref7_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref7 Frame Sync Edge Control	See description for registers at address 0x0D8

Register_Address: **0x0E0**
Register Name: **ref8_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref8 Frame Sync Edge Control	See description for registers at address 0x0D8

Register_Address: **0x0E1**
Register Name: **ref9_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref9 Frame Sync Edge Control	See description for registers at address 0x0D8

Register_Address: **0x0E2**
Register Name: **ref10_sync_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	Ref10 Frame Sync Edge Control	See description for registers at address 0x0D8

Register_Address: **0x0E3**
Register Name: **dpll0_psl_decay_time**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL0 PSL decay time	This register is used to specify the time interval between instants when the exponentially decaying PSL value is computed. This register contains the exponent which when plugged in the following function provides the desired time interval in milliseconds: Decay Time Interval (ms) =0.14336*(2 ^ **dpll0_psl_decay_time)** A register value of zero defaults to 9, giving a decay time interval of 73.4 ms

Register_Address: **0x0E4**
Register Name: **dpll1_psl_decay_time**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL1 PSL decay time	See description for registers at address 0x0E3

Register_Address: **0x0E5**
Register Name: **dpll2_psl_decay_time**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL2 PSL decay time	See description for registers at address 0x0E3

Register_Address: **0x0E6**
Register Name: **dpll3_psl_decay_time**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL3 PSL decay time	See description for registers at address 0x0E3

Register_Address: **0x0E7**
Register Name: **dpll0_psl_scaling**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL0 PSL scaling	This register is used to specify the scaling factor with which to scale the PSL. The scaling factor is computed as follows: PSL Scaling Factor = **dpll0_psl_scaling**/256 The host can program any value from 1 to 255, giving scaling factors from 0.0039 to 0.996 respectively. A register value of zero defaults to a scaling factor of 0.9 (equivalent to the scaling factor selected by value of 0xE6).

Register_Address: **0x0E8**
Register Name: **dpll1_psl_scaling**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL1 PSL scaling	See description for 0x0E7

Register_Address: **0x0E9**
Register Name: **dpll2_psl_scaling**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL2 PSL scaling	See description for 0x0E7

Register_Address: **0x0EA**
Register Name: **dpll3_psl_scaling**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL3 PSL scaling	See description for 0x0E7

Register_Address: **0x0EC**
Register Name:**ref_1_0_clk_sync_pair**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Enables clock/sync pair and specifies frame pulse input reference 1	When these four bits are set to the same number as the corresponding reference (in case of Ref 1, this is 0x1), the reference does not have corresponding sync pulse. When these bits are programmed from 0x0 to 0xA (0x1 excluded), they specify an input reference on which a sync pulse is fed. For example, a value of 0x5 specify that sync pulse is input on the Ref 5. If the one of DPLLs is programmed to be locked to Ref 1, the DPLL will lock to Ref 1 but its output frame pulses and clocks will be phase aligned to the frame pulse at input from the Ref 5. Values 0xB, 0xC, 0xD, 0xE are reserved.
3:0	Enables clock/sync pair and specifies frame pulse input reference 0	For description see bits 7:4 above

Register_Address: **0x0ED**
Register Name:**ref_3_2_clk_sync_pair**
Default Value: **0x32**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Enables clock/sync pair and specifies frame pulse input reference 3	See description for register at address 0x0EC bits 7:4
3:0	Enables clock/sync pair and specifies frame pulse input reference 2	See description for register at address 0x0EC bits 7:4

Register_Address: **0x0EE**
Register Name:**ref_5_4_clk_sync_pair**
Default Value: **0x54**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Enables clock/sync pair and specifies frame pulse input reference 5	See description for register at address 0x0EC bits 7:4
3:0	Enables clock/sync pair and specifies frame pulse input reference 4	See description for register at address 0x0EC bits 7:4

Register_Address: **0x0EF**
Register Name:**ref_7_6_clk_sync_pair**
Default Value: **0x76**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Enables clock/sync pair and specifies frame pulse input reference 7	See description for register at address 0x0EC bits 7:4
3:0	Enables clock/sync pair and specifies frame pulse input reference 6	See description for register at address 0x0EC bits 7:4

Register_Address: **0x0F0**
Register Name:**ref_9_8_clk_sync_pair**
Default Value: **0x98**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Enables clock/sync pair and specifies frame pulse input reference 9	See description for register at address 0x0EC bits 7:4
3:0	Enables clock/sync pair and specifies frame pulse input reference 8	See description for register at address 0x0EC bits 7:4

Register_Address: **0x0F1**
Register Name:**ref_10_clk_sync_pair**
Default Value: **0x0A**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Enables clock/sync pair and specifies frame pulse input reference 10	See description for register at address 0x0EC bits 7:4

Register_Address: **0x0FF**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	SPI Page Selection register	Unsigned binary value of these bits represents selected page for SPI access. See register at address 0x07F for details

Register_Address: **0x100**
Register Name: **dpll0_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
7:5	DPLL loop filter corner frequency selection	These bits control DPLL0 loop filter corner frequency. Bit selection: 000 = 14 Hz 001 = 28 Hz 010 = 56 Hz 011 = 112 Hz 100 = 224 Hz 101 = 448 Hz 110 = 896 Hz 111 = programmable bandwidth based on DPLL0 Variable Bandwidth Selection register (dpll0_var_bw_sel)

Register_Address: **0x100**
Register Name: **dpll0_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
4	Time Interval Error (TIE) clear enable	This bit controls the DPLL0 output to input alignment. When this bit is set to high, the DPLL0 will align its outputs to the reset position (specified by appropriate phase shift selection). This bit should be set when initial output to input alignment is desired after numerous reference rearrangement. To achieve 'hitless' reference switch, this bit has to be kept low.
3:2	Phase Slope Limit	These bits control DPLL0 phase slope limiter. Bit selection: 00 = 61 usec/sec 01 = 7.5 usec/sec 10 = 0.885 usec/sec 11 = unlimited
1:0	Reserved	Leave as default

Register_Address: **0x101**
Register Name: **dpll0_var_bw_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL0 variable low bandwidth selection	When DPLL0 loop filter corner frequency selection is programmed to '111', these bits specify DPLL0 corner frequency as per the following formula, using E32 series style: Value = round(32 * log(BandWidth*10^4)), where BandWidth is given in Hz **Example:** if desired frequency is 100 uHz, value to be written to this register is 0x00, for 1Hz the value is 0x80 and so on. The maximum loop bandwidth that can be programmed in this register is 13 Hz.

Register_Address: **0x102**
Register Name: **dpll0_pull_in_hold_in**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2:0	DPLL0 Pull-in Hold-in selection register	These bits control DPLL0 pull-in / hold-in range selection. Bit selection: 000 = +/- 12 ppm 001 = +/- 52 ppm 010 = +/- 83 ppm 011 = +/- 130 ppm 100 = +/- 400 ppm 101 = reserved 110 = reserved 111 = unlimited

Register_Address: **0x103**
Register Name: **dpll0_mode_refsel**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reference selection	When the 'DPLL0 mode' bits of this register (bits 2:0) are set to '10' (forced reference mode), these bits specify which reference the DPLL0 is forced to select. When the forced reference fails, the DPLL0 will go into holdover mode When the 'DPLL0 mode' bits of this register are other than forced reference mode, these bits are ignored.
3	External feedback enable	When this bit is set, the DPLL0 will use the external feedback phase to compensate for the delay on all related output clocks (all output clocks coming from all synthesizers that are associated with the DPLL0). When this bit is 0, DPLL0 will ignore external feedback. **Note 1:** There is only one external feedback available, so the external feedback phase will be used if this bit is set, regardless whether DPLL0 is used to create the external feedback phase or one of other DPLLs. **Note 2:** Bit 7 in the External Feedback Control Register (register 0x181) should be programmed after programming this bit. Otherwise, input to output misalignment can be expected.

Register_Address: **0x103**
Register Name: **dpll0_mode_refsel**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
2:0	DPLL0 Mode	These bits determine DPLL0 mode of operation. Selection: 000 = freerun mode 001 = forced holdover mode 010 = forced reference lock mode 011 = automatic mode 100 = NCO mode 101, 110, 111 = reserved For more information on these modes of operation, please see Section 4.3.2, “DPLL Modes“ on page 21.

Register_Address: **0x104**
Register Name: **dpll0_refsel_stat**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Selected reference status	When the 'DPLL0 mode' bits of the dpll0_mode_refsel register are set to '11' (automatic mode), these bits represent the selected reference status, i.e. '0000' = Ref0, '0001' = Ref1 and so on.

Register_Address: **0x105**
Register Name: **dpll0_ref_priority1_0**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref1	When the DPLL0 is in automatic mode of operation programmed in the DPLL0 Mode field in dpll_mode_refsel , these bits are used to select priority of Ref1 for DPLL. 0000 is highest priority and 1110 is lowest priority. Setting these bits to 1111 will disable Ref1 reference (that will prevent DPLL0 from locking to Ref1). When references are programmed to have different priority number, the DPLL0 will perform 'REVERTIVE' switching between them. This means that the DPLL0 will always switch to the highest priority reference available with lowest priority number) when that reference becomes available (input is valid). When two or more input references are programmed to have same priority number, the DPLL0 will perform 'NON-REVERTIVE' switching between them. This means that the DPLL0 will not perform a switch to another reference with the same priority when that reference becomes available. Combinations of the same and different priority numbers can be used, such that the DPLL0 performs revertive switching between different priority references, but non-revertive switching among references with the same priority. Example: if Ref0 has priority 0 (highest), Ref1, Ref2 and Ref3 have priority 1. Whenever Ref0 becomes available, DPLL0 will switch to it. But, if Ref0 is not available, DPLL0 will remain locking to currently selected reference (e.g. Ref3) even when Ref1 or Ref2 become available.
3:0	priority selection Ref0	See description for bits 7:4 above

Register_Address: **0x106**
Register Name: **dpll0_ref_priority3_2**
Default Value: **0x32**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref3	See description for register at address 0x105
3:0	priority selection Ref2	See description for register at address 0x105

Register_Address: **0x107**
Register Name: **dpll0_ref_priority5_4**
Default Value: **0x54**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref5	See description for register at address 0x105
3:0	priority selection Ref4	See description for register at address 0x105

Register_Address: **0x108**
Register Name: **dpll0_ref_priority7_6**
Default Value: **0x76**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref7	See description for register at address 0x105
3:0	priority selection Ref6	See description for register at address 0x105

Register_Address: **0x109**
Register Name: **dpll0_ref_priority9_8**
Default Value: **0x98**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref9	See description for register at address 0x105
3:0	priority selection Ref8	See description for register at address 0x105

Register_Address: **0x10A**
Register Name: **dpll0_ref_priority10**
Default Value: **0x0A**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	priority selection Ref10	See description for register at address 0x105

Register_Address: **0x10B:0x10C**
Register Name: **dpll0_psl_max_phase**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	DPLL0 PSL Max Phase	This register is used to specify the maximum phase for which the phase slope will stay below specified PSL. Selection: 0: Maximum phase step while meeting the phase slope limit will be 10 us (default) 1 ≤ **dpll0_psl_max_phase** ≤1000: Maximum phase step(us) = 0.1***dpll0_psl_max_phase** 1000 < **dpll0_psl_max_phase** ≤ 65535: Same as 1000 (100us) **Note:** For phase steps above the maximum phase, the DPLL will operate correctly but not guarantee that it will meet the given phase slope limit in **dpll0_ctrl**.

Register_Address: **0x10D**
Register Name: **dpll0_ref_fail_mask**
Default Value: **0x87**
Type:**R/W**

Bit Field	Function Name	Description
7	refswitch mask GST	When set high, this bit allows the selected reference GST failure to cause the DPLL0 to perform a reference switch. When set low, the selected reference GST failure will be masked and DPLL0 will not perform a reference switch due to a GST failure. 0 = mask 1 = enable (activate)
6	refswitch mask CFM	When set high, this bit allows the selected reference CFM failure to cause DPLL0 to perform a reference switch. When low, the selected reference CFM failure will be masked and DPLL0 will not perform a reference switch due to a CFM failure. 0 = mask 1 = enable (activate)
5	refswitch mask SCM	When set high, this bit allows the selected reference SCM failure to cause DPLL0 to perform a reference switch. When low, the selected reference SCM failure will be masked and DPLL0 will not perform a reference switch due to a SCM failure. 0 = mask 1 = enable (activate)
4	refswitch mask LOS	When set high, this bit allows the selected reference LOS failure to cause DPLL0 to perform reference switch. When low, the selected reference LOS failure will be masked and DPLL0 will not perform a reference switch due to a LOS failure. 0 = mask 1 = enable (activate)
3	holdover mask GST	When set high, this bit allows the selected reference GST failure to cause DPLL0 to go into holdover. When low, the selected reference GST failure will be masked and DPLL0 will not go into holdover due to a GST failure. 0 = mask 1 = enable (activate) **Note:** This bit should never be programmed to 1 if neither 'holdover mask CFM' nor 'holdover mask SCM' bit is programmed to 1 (e.g. bits 3:1 should never be programmed to '100').
2	holdover mask CFM	When set high, this bit allows the selected reference CFM failure to cause DPLL0 to go into holdover. When low, the selected reference CFM failure will be masked and DPLL0 will not go into holdover due to a CFM failure. 0 = mask 1 = enable (activate)

Register_Address: **0x10D**
Register Name: **dpll0_ref_fail_mask**
Default Value: **0x87**
Type:**R/W**

Bit Field	Function Name	Description
1	holdover mask SCM	When set high, this bit allows the selected reference SCM failure to cause DPLL0 to go into holdover. When low, the selected reference SCM failure will be masked and DPLL0 will not go into holdover due to a SCM failure. 0 = mask 1 = enable (activate)
0	holdover mask LOS	When set high, this bit allows the selected reference external LOS signal to cause DPLL0 to go into holdover. When low, selected reference external LOS signal will be masked and DPLL0 will not go to holdover when the LOS signal is active high. 0 = mask 1 = enable (activate)

Register_Address: **0x10E**
Register Name: **dpll0_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	refswitch mask PFM	When set high, this bit allows selected reference PFM failure to cause DPLL0 to perform a reference switch. When low, selected reference PFM failure will be masked and DPLL0 will not perform reference switch due to a PFM failure.
3:1	Reserved	Leave as default
0	holdover mask PFM	When set high, this bit allows selected reference PFM failure to cause DPLL0 to go into holdover. When low, selected reference PFM failure will be masked and DPLL0 will not go ino holdover due to the PFM failure.

Register_Address: **0x10F**
Register Name: **dpll0_ho_edge_sel**
Default Value: **0x0B**
Type:**R/W**

Bit Field	Function Name	Description
7:6	DPLL0 reference edge selection	These bits define the selected reference edge sensitivity 00 = positive (rising) edge 01 = negative (falling) edge 10 = low pulse 11 = high pulse The low pulse and the high pulse options select a middle sample point halfway between the clock edges.
5	reserved	Leave as default
4:0	DPLL0 holdover storage delay	These bits specify the DPLL0 holdover storage delay as per the following formula, using E8 series style: Value = round(8 * log(StorageDelay/10)), where StorageDelay is given in ms Example, if desired delay is 10ms, value to be written to this register is 0x00, for 1 second the value is 0x10, while for 75 seconds the value is 0x1F The default value of 0xB provides a storage delay of 237 ms.

Register_Address: **0x110**
Register Name: **dpll0_pbo_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2	Reset PBO Magnitude	When set high, the measurement of total accumulated phase between input and output due to phase build out is enabled. When set low, a measurement of total accumulated phase is reset to zero.

Register_Address: **0x110**
Register Name: **dpll0_pbo_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
1	Reset PBO Count	When set high, the counter is enabled and counts phase build out occurrences. When set low, the counter which indicates number of phase build out occurrences is reset to zero.
0	PBO enable	When set high, phase build out feature is enabled. When set low the phase build out feature is disabled.

Register_Address: **0x111**
Register Name: **dpll0_pbo_jitter_th_ctrl**
Default Value: **0x23**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Minimum phase error threshold	Sets minimum phase error threshold from 0 to 25.5 us with resolution of 100ns.When this threshold is exceeded, the device will assume that phase error is not due to jitter but due to phase transient. If this transient then exceeds the limit specified in register **dpll0_pbo_mini_slope_th** (address 0x112), the device will perform phase build out.

Register_Address: **0x112**
Register Name: **dpll0_pbo_min_slope_th**
Default Value: **0x70**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Minimum phase transient slope threshold	Sets minimum phase transient slope threshold from 0 to 2.55us/0.1s in steps of 10ns/0.1s. When this threshold is exceeded, and when condition in register **dpll0_pbo_jitter_th_ctrl** at address 0x111 is met, the device will perform phase build out. Default value is1.12us/0.1s (0x70)

Register_Address: **0x113**
Register Name: **dpll0_pbo_end_interval**
Default Value: **0x20**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Transient interval duration	Sets the time, after which if no minimum slope interval is exceeded the transient is considered finished. Interval range is from 0 to 2.55 s in steps of 10 ms. Default value is 320ms

Register_Address: **0x114**
Register Name: **dpll0_pbo_time_out**
Default Value: **0x64**
Type:**R/W**

Bit Field	Function Name	Description
7:0	PBO timeout interval	Sets the PBO timeout interval, after which, if the minimum slope interval continues to be exceeded, the dpll will not perform a phase build-out; otherwise, the dpll will perform a phase build-out.The valid range is 0 to 2.55 s in steps of 10ms. Default is 1s (0x64). When set to 0x00, the timeout circuit is disabled.

Register_Address: **0x115**
Register Name: **dpll0_pbo_counter**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:0	PBO counter	The register contains the number of phase build out occurrences. When it reaches 255, the counter will not overflow. To reset the counter the field "Reset PBO Count" is set low in register dpll_pbo_ctrl (address 0x110)

Register_Address: **0x116:0x118**
Register Name: **dpll0_pbo_magnitude**
Default Value: **0x000000**
Type:**R**

Bit Field	Function Name	Description
23:0	PBO magnitude	This register contains 2s complement value of cumulative phase difference during phase build out occurrences. The range is +/- 8.39 ms in steps of 1 ns.To reset the value see 'Reset PBO Magnitude' in register dpll_pbo_ctrl (address 0x110)

Register_Address: **0x119**
Register Name: **dpll0_damping_ctrl**
Default Value: **0x05**
Type:R/W

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Damping Factor	This register controls the damping factor, Selection: 0x2 - For use when pulling into a 1 Hz reference and 1 mHz or 30 mHz bandwidths as explained in "DPLL bandwidth (jitter/wander transfer)" on page 20 0x5 - default (Recommended for all application except as noted above) All other values reserved **Note:** A damping factor of 5 corresponds to a gain peaking of less than 0.1 dB.

Register_Address: **0x120**
Register Name: **dpll1_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
7:5	DPLL1 loop filter corner frequency selection	See description for register at address 0x100

Register_Address: **0x120**
Register Name: **dpll1_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
4	Time Interval Error (TIE) clear enable	See description for register at address 0x100
3:2	Phase Slope Limit	See description for register at address 0x100
1:0	Reserved	Leave as default

Register_Address: **0x121**
Register Name: **dpll1_var_bw_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL1 variable bandwidth selection	See description for register at address 0x101

Register_Address: **0x122**
Register Name: **dpll1_pull_in_hold_in**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2:0	DPLL1 Pull-in Hold-in selection register	See description for register at address 0x102

Register_Address: **0x123**
Register Name: **dpll1_mode_refsel**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reference selection	See description for register at address 0x103
3	External feedback enable	See description for register at address 0x103
2:0	DPLL1 Mode	See description for register at address 0x103

Register_Address: **0x124**
Register Name: **dpll1_refsel_stat**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Selected reference status	See description for register at address 0x104

Register_Address: **0x125**
Register Name: **dpll1_ref_priority1_0**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref1	See description for register at address 0x105
3:0	priority selection Ref0	See description for register at address 0x105

Register_Address: **0x126**
Register Name: **dpll1_ref_priority3_2**
Default Value: **0x32**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref3	See description for register at address 0x105
3:0	priority selection Ref2	See description for register at address 0x105

Register_Address: **0x127**
Register Name: **dpll1_ref_priority5_4**
Default Value: **0x54**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref5	See description for register at address 0x105
3:0	priority selection Ref4	See description for register at address 0x105

Register_Address: **0x128**
Register Name: **dpll0_ref_priority7_6**
Default Value: **0x76**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref7	See description for register at address 0x105
3:0	priority selection Ref6	See description for register at address 0x105

Register_Address: **0x129**
Register Name: **dpll1_ref_priority9_8**
Default Value: **0x98**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref9	See description for register at address 0x105
3:0	priority selection Ref8	See description for register at address 0x105

Register_Address: **0x12A**
Register Name: **dpll1_ref_priority10**
Default Value: **0x0A**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	priority selection Ref10	See description for register at address 0x105

Register_Address: **0x12B:0x12C**
Register Name: **dpll1_psl_max_phase**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	DPLL1 PSL Max Phase	See description for register at address 0x10B:0x10C

Register_Address: **0x12D**
Register Name: **dpll1_ref_fail_mask**
Default Value: **0x87**
Type:**R/W**

Bit Field	Function Name	Description
7	refswitch mask GST	See description for register at address 0x10D
6	refswitch mask CFM	See description for register at address 0x10D
5	refswitch mask SCM	See description for register at address 0x10D
4	refswitch mask LOS	See description for register at address 0x10D
3	holdover mask GST	See description for register at address 0x10D
2	holdover mask CFM	See description for register at address 0x10D
1	holdover mask SCM	See description for register at address 0x10D
0	holdover mask LOS	See description for register at address 0x10D

Register_Address: **0x12E**
Register Name: **dpll1_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	refswitch mask PFM	See description for register at address 0x10E
3:1	Reserved	Leave as default
0	holdover mask PFM	See description for register at address 0x10E

Register_Address: **0x12F**
Register Name: **dpll1_ho_edge_sel**
Default Value: **0x0B**
Type:**R/W**

Bit Field	Function Name	Description
7:6	DPLL1 reference edge selection	See description for register at address 0x10F
5	Reserved	Leave as default
4:0	DPLL1 holdover storage delay	See description for register at address 0x10F

Register_Address: **0x130**
Register Name: **dpll1_pbo_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2	Reset PBO Magnitude	See description for register at address 0x110
1	Reset PBO Count	See description for register at address 0x110
0	PBO enable	See description for register at address 0x110

Register_Address: **0x131**
Register Name: **dpll1_pbo_jitter_th_ctrl**
Default Value: **0x23**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Minimum phase error threshold	See description for register at address 0x111

Register_Address: **0x132**
Register Name: **dpll1_pbo_min_slope_th**
Default Value: **0x70**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Minimum phase transient slope threshold	See description for register at address 0x112

Register_Address: **0x133**
Register Name: **dpll1_pbo_end_interval**
Default Value: **0x20**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Transient interval duration	See description for register at address 0x113

Register_Address: **0x134**
Register Name: **dpll1_pbo_time_out**
Default Value: **0x64**
Type:**R/W**

Bit Field	Function Name	Description
7:0	PBO timeout interval	See description for register at address 0x114

Register_Address: **0x135**
Register Name: **dpll1_pbo_counter**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:0	PBO counter	See description for register at address 0x115

Register_Address: **0x136:0x138**
Register Name: **dpll1_pbo_magnitude**
Default Value: **0x000000**
Type:**R**

Bit Field	Function Name	Description
23:0	PBO magnitude	See description for register at address 0x116:0x118

Register_Address: **0x139**
Register Name: **dpll1_damping_ctrl**
Default Value: **0x05**
Type:R/W

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Damping Factor	See description for register at address 0x119

Register_Address: **0x140**
Register Name: **dpll2_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
7:5	DPLL2 loop filter corner frequency selection	See description for register at address 0x100
4	Time Interval Error (TIE) clear enable	See description for register at address 0x100
3:2	Phase Slope Limit	See description for register at address 0x100
1:0	Reserved	Leave as default

Register_Address: **0x141**
Register Name: **dpll2_var_bw_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL2 variable bandwidth selection	See description for register at address 0x101

Register_Address: **0x142**
Register Name: **dpll2_pull_in_hold_in**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
7:0	DPLL2 Pull-in Hold-in selection register	See description for register at address 0x102

Register_Address: **0x143**
Register Name: **dpll2_mode_refsel**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reference selection	See description for register at address 0x103
3	External feedback enable	See description for register at address 0x103
2:0	DPLL2 Mode	See description for register at address 0x103

Register_Address: **0x144**
Register Name: **dpll2_refsel_stat**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Selected reference status	See description for register at address 0x104

Register_Address: **0x145**
Register Name: **dpll2_ref_priority1_0**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref1	See description for register at address 0x105
3:0	priority selection Ref0	See description for register at address 0x105

Register_Address: **0x146**
Register Name: **dpll2_ref_priority3_2**
Default Value: **0x32**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref3	See description for register at address 0x105
3:0	priority selection Ref2	See description for register at address 0x105

Register_Address: **0x147**
Register Name: **dpll2_ref_priority5_4**
Default Value: **0x54**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref5	See description for register at address 0x105
3:0	priority selection Ref4	See description for register at address 0x105

Register_Address: **0x148**
Register Name: **dpll2_ref_priority7_6**
Default Value: **0x76**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref7	See description for register at address 0x105
3:0	priority selection Ref6	See description for register at address 0x105

Register_Address: **0x149**
Register Name: **dpll2_ref_priority9_8**
Default Value: **0x98**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref9	See description for register at address 0x105
3:0	priority selection Ref8	See description for register at address 0x105

Register_Address: **0x14A**
Register Name: **dpll2_ref_priority10**
Default Value: **0x0A**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	priority selection Ref10	See description for register at address 0x105

Register_Address: **0x14B:0x14C**
Register Name: **dpll2_psl_max_phase**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	DPLL2 PSL Max Phase	See description for register at address 0x10B:0x10C

Register_Address: **0x14D**
Register Name: **dpll2_ref_fail_mask**
Default Value: **0x87**
Type:**R/W**

Bit Field	Function Name	Description
7	refswitch mask GST	See description for register at address 0x10D
6	refswitch mask CFM	See description for register at address 0x10D
5	refswitch mask SCM	See description for register at address 0x10D
4	refswitch mask LOS	See description for register at address 0x10D
3	holdover mask GST	See description for register at address 0x10D
2	holdover mask CFM	See description for register at address 0x10D
1	holdover mask SCM	See description for register at address 0x10D
0	holdover mask LOS	See description for register at address 0x10D

Register_Address: **0x14E**
Register Name: **dpll2_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	refswitch mask PFM	See description for register at address 0x10E
3:1	Reserved	Leave as default
0	holdover mask PFM	See description for register at address 0x10E

Register_Address: **0x14F**
Register Name: **dpll2_ho_edge_sel**
Default Value: **0x0B**
Type:**R/W**

Bit Field	Function Name	Description
7:6	DPLL2 reference edge selection	See description for register at address 0x10F
5	Reserved	Leave as default
4:0	DPLL2 holdover storage delay	See description for register at address 0x10F

Register_Address: **0x150**
Register Name: **dpll2_pbo_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	reserved	Leave as default
2	Reset PBO Magnitude	See description for register at address 0x110
1	Reset PBO Count	See description for register at address 0x110
0	PBO enable	See description for register at address 0x110

Register_Address: **0x151**
Register Name: **dpll2_pbo_jitter_th_ctrl**
Default Value: **0x23**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Minimum phase error threshold	See description for register at address 0x111

Register_Address: **0x152**
Register Name: **dpll2_pbo_min_slope_th**
Default Value: **0x70**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Minimum phase transient slope threshold	See description for register at address 0x112

Register_Address: **0x153**
Register Name: **dpll2_pbo_end_interval**
Default Value: **0x20**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Transient interval duration	See description for register at address 0x113

Register_Address: **0x154**
Register Name: **dpll2_pbo_time_out**
Default Value: **0x64**
Type:**R/W**

Bit Field	Function Name	Description
7:0	PBO timeout interval	See description for register at address 0x114

Register_Address: **0x155**
Register Name: **dpll2_pbo_counter**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:0	PBO counter	See description for register at address 0x115

Register_Address: **0x156:0x158**
Register Name: **dpll2_pbo_magnitude**
Default Value: **0x000000**
Type:**R**

Bit Field	Function Name	Description
23:0	PBO magnitude	See description for register at address 0x116:118

Register_Address: **0x159**
Register Name: **dpll2_damping_ctrl**
Default Value: **0x05**
Type:R/W

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Damping Factor	See description for register at address 0x119

Register_Address: **0x160**
Register Name: **dpll3_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
7:5	DPLL3 loop filter corner frequency selection	See description for register at address 0x100
4	Time Interval Error (TIE) clear enable	See description for register at address 0x100
3:2	Phase Slope Limit	See description for register at address 0x100
1:0	Reserved	Leave as default

Register_Address: **0x161**
Register Name: **dpll3_var_bw_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL3 variable bandwidth selection	See description for register at address 0x101

Register_Address: **0x162**
Register Name: **dpll3_pull_in_hold_in**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2:0	DPLL3 Pull-in Hold-in selection register	See description for register at address 0x102

Register_Address: **0x163**
Register Name: **dpll3_mode_refsel**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reference selection	See description for register at address 0x103
3	External feedback enable	See description for register at address 0x103
2:0	DPLL3 Mode	See description for register at address 0x103

Register_Address: **0x164**
Register Name: **dpll3_refsel_stat**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Selected reference status	See description for register at address 0x104

Register_Address: **0x165**
Register Name: **dpll3_ref_priority1_0**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref1	See description for register at address 0x105
3:0	priority selection Ref0	See description for register at address 0x105

Register_Address: **0x166**
Register Name: **dpll3_ref_priority3_2**
Default Value: **0x32**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref3	See description for register at address 0x105
3:0	priority selection Ref2	See description for register at address 0x105

Register_Address: **0x167**
Register Name: **dpll3_ref_priority5_4**
Default Value: **0x54**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref5	See description for register at address 0x105
3:0	priority selection Ref4	See description for register at address 0x105

Register_Address: **0x168**
Register Name: **dpll3_ref_priority7_6**
Default Value: **0x76**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref7	See description for register at address 0x105
3:0	priority selection Ref6	See description for register at address 0x105

Register_Address: **0x169**
Register Name: **dpll3_ref_priority9_8**
Default Value: **0x98**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref9	See description for register at address 0x105
3:0	priority selection Ref8	See description for register at address 0x105

Register_Address: **0x16A**
Register Name: **dpll3_ref_priority10**
Default Value: **0x0A**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	priority selection Ref10	See description for register at address 0x105

Register_Address: **0x16B:0x16C**
Register Name: **dpll3_psl_max_phase**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:0	DPLL3 PSL Max Phase	See description for register at address 0x10B:0x10C

Register_Address: **0x16D**
Register Name: **dpll3_ref_fail_mask**
Default Value: **0x87**
Type:**R/W**

Bit Field	Function Name	Description
7	refswitch mask GST	See description for register at address 0x10D
6	refswitch mask CFM	See description for register at address 0x10D
5	refswitch mask SCM	See description for register at address 0x10D
4	refswitch mask LOS	See description for register at address 0x10D
3	holdover mask GST	See description for register at address 0x10D
2	holdover mask CFM	See description for register at address 0x10D
1	holdover mask SCM	See description for register at address 0x10D
0	holdover mask LOS	See description for register at address 0x10D

Register_Address: **0x16E**
Register Name: **dpll3_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	refswitch mask PFM	See description for register at address 0x10E
3:1	Reserved	Leave as default
0	holdover mask PFM	See description for register at address 0x10E

Register_Address: **0x16F**
Register Name: **dpll3_ho_edge_sel**
Default Value: **0x0B**
Type:**R/W**

Bit Field	Function Name	Description
7:6	DPLL3 reference edge selection	See description for register at address 0x10F
5	Reserved	Leave as default
4:0	DPLL3 holdover storage delay	See description for register at address 0x10F

Register_Address: **0x170**
Register Name: **dpll3_pbo_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	reserved	Leave as default
2	Reset PBO Magnitude	See description for register at address 0x110
1	Reset PBO Count	See description for register at address 0x110
0	PBO enable	See description for register at address 0x110

Register_Address: **0x171**
Register Name: **dpll3_pbo_jitter_th_ctrl**
Default Value: **0x23**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Minimum phase error threshold	See description for register at address 0x111

Register_Address: **0x172**
Register Name: **dpll3_pbo_min_slope_th**
Default Value: **0x70**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Minimum phase transient slope threshold.	See description for register at address 0x112

Register_Address: **0x173**
Register Name: **dpll3_pbo_end_interval**
Default Value: **0x20**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Transient interval duration	See description for register at address 0x113

Register_Address: **0x174**
Register Name: **dpll3_pbo_time_out**
Default Value: **0x64**
Type:**R/W**

Bit Field	Function Name	Description
7:0	PBO timeout interval	See description for register at address 0x114

Register_Address: **0x175**
Register Name: **dpll3_pbo_counter**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:0	PBO counter	See description for register at address 0x115

Register_Address: **0x176:0x178**
Register Name: **dpll3_pbo_magnitude**
Default Value: **0x000000**
Type:**R**

Bit Field	Function Name	Description
23:0	PBO magnitude	See description for register at address 0x116:0x118

Register_Address: **0x17F**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Page Selection register	See description for register at address 0x7F

Register_Address: **0x179**
Register Name: **dpll3_damping_ctrl**
Default Value: **0x05**
Type:R/W

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Damping Factor	See description for register at address 0x119

Register_Address: **0x180**
Register Name: **dpll_hold_lock_status**
Default Value: **0x00**
Type::**StickyR/W**

Bit Field	Function Name	Description
7	DPLL3 lock status	When DPLL3 is locked to a reference, the device will set this bit high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever DPLL3, it will be set regardless of any mask bits.

Register_Address: **0x180**
Register Name: **dpll_hold_lock_status**
Default Value: **0x00**
Type::**StickyR/W**

Bit Field	Function Name	Description
6	DPLL3 holdover status	This bit is set high when DPLL3 is in holdover mode. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever DPLL3 is in holdover, it will be set regardless of any mask bits.
5	DPLL2 lock status	When DPLL2 is locked to a reference, the device will set this bit high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever DPLL2, it will be set regardless of any mask bits.
4	DPLL2 holdover status	This bit is set high when DPLL2 is in holdover mode. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever DPLL2 is in holdover, it will be set regardless of any mask bits.
3	DPLL1 lock status	When DPLL1 is locked to a reference, the device will set this bit high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever DPLL1, it will be set regardless of any mask bits.
2	DPLL1 holdover status	This bit is set high when DPLL1 is in holdover mode. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever DPLL1 is in holdover, it will be set regardless of any mask bits.
1	DPLL0 lock status	When DPLL0 is locked to a reference, the device will set this bit high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever DPLL0, it will be set regardless of any mask bits.
0	DPLL0 holdover status	This bit is set high when DPLL0 is in holdover mode. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever DPLL0 is in holdover, it will be set regardless of any mask bits.

Register_Address: **0x181**
Register Name: **ext_fb_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	External feedback enable	When this bit is set to 1, External feedback is enabled **Note:** This bit should be set last in the process of configuring external feedback.
6	Reserved	Leave as default
5:2	External feedback source	Specifies the reference to be used as the external feedback source input. 0000 = ref0 0001 = ref1 ... 1010 = ref10 1011-1111 = reserved **Note:** In order to have proper behaviour when external feedback is enabled, it is required that the main reference and the external feedback source are frequency locked (they do not have to have the same carrier frequency).
1:0	External feedback DPLL selection	Specifies the DPLL to be used for the external feedback feature. The DPLL selected is used for determining the phase difference between its input reference and the selected feedback source. ‘00‘ - DPLL0 ‘01‘ - DPLL1 ‘10‘ - DPLL2 ‘11‘ - DPLL3 **Note:** If external feedback is enabled for particular DPLL ('external feedback enable' bit of the 'dpll_mode_refsel' register is set), the resulting DPLL output phase will be compensated for the external feedback phase, regardless of which DPLL is used for the external feedback phase calculation.

Register_Address: **0x182**
Register Name: **dpll_config**
Default Value: **0x04**
Type: **R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default

Register_Address: **0x182**
Register Name: **dpll_config**
Default Value: **0x04**
Type: **R/W**

Bit Field	Function Name	Description
2:0	DPLL Configuration	Selects which DPLLs are enabled Selection: 000 = none 001 = DPLL0 010 = DPLL0 and DPLL1 011 = DPLL0, DPLL1 and DPLL2 100 = all four DPLLs are enabled 101-111 = reserved

Register_Address: **0x183**
Register Name: **dpll_lock_selection**
Default Value: **0x00**
Type:R/W

Bit Field	Function Name	Description
7:6	DPLL3 lock selection	These bits select DPLL3 lock indicator condition (appearing in the dpll_hold_lock_status register). Selection: 00 = phase error is smaller than 36 us during 10 s 01 = phase error is smaller than 1 us during 1 s 10 = phase error is smaller than 10 us during 1 s 11 = phase error is smaller than 10 us during 10 s
5:4	DPLL2 lock selection	These bits select DPLL2 lock indicator condition (appearing in the dpll_hold_lock_status register). Selection: 00 = phase error is smaller than 36 us during 10 s 01 = phase error is smaller than 1 us during 1 s 10 = phase error is smaller than 10 us during 1 s 11 = phase error is smaller than 10 us during 10 s
3:2	DPLL1 lock selection	These bits select DPLL1 lock indicator condition (appearing in the dpll_hold_lock_status register). Selection: 00 = phase error is smaller than 36 us during 10 s 01 = phase error is smaller than 1 us during 1 s 10 = phase error is smaller than 10 us during 1 s 11 = phase error is smaller than 10 us during 10 s

Register_Address: **0x183**
Register Name: **dpll_lock_selection**
Default Value: **0x00**
Type:R/W

Bit Field	Function Name	Description
1:0	DPLL0 lock selection	These bits select DPLL0 lock indicator condition (appearing in the dpll_hold_lock_status register). Selection: 00 = phase error is smaller than 36 us during 10 s 01 = phase error is smaller than 1 us during 1 s 10 = phase error is smaller than 10 us during 1 s 11 = phase error is smaller than 10 us during 10 s

Register_Address: **0x18D:0x191**
Register Name: **dpll0_df_offset**
Default Value: **0x0000000000**
Type: **R/W**

Bit Field	Function Name	Description
39:0	NCO0 Delta Frequency offset	When DPLL0 is programmed into NCO0 mode (dpll0_mode_refsel register), this register contains a 2's complement binary value of delta frequency offset. This register controls delta frequency of Synthesizers that are associated with the DPLL0/NCO0. Delta frequency is expressed in steps of +/- 2^-40 of nominal setting. The output frequency should be calculated as per formula: f_out = (1 - X/2^40)*f_nom where, X is 2's complement number specified in this register, f_nom is the nominal frequency set by Bs, Ks, Ms, Ns and postdivider number for particular Synthesizer and f_out is the desired output frequency **Note 1:** Delta frequency offset combined with the Synthesizer Frequency should be between 1.0 GHz and 1.5 GHz. **Note 2:** The delta frequency offset should not exceed +/-2% of the nominal value. **Note 3:** The delta frequency offset should not be changed by more than 7 ppm in a single update.

Register_Address: **0x192:0x196**
Register Name: **dpll1_df_offset**
Default Value: **0x0000000000**
Type: **R/W**

Bit Field	Function Name	Description
39:0	NCO1 Delta Frequency offset	See description of the register at address 0x18D:0x191

Register_Address: **0x197:0x19B**
Register Name: **dpll2_df_offset**
Default Value: **0x0000000000**
Type: **R/W**

Bit Field	Function Name	Description
39:0	NCO2 Delta Frequency offset	See description of the register at address 0x18D:0x191

Register_Address: **0x19C:0x1A0**
Register Name: **dpll3_df_offset**
Default Value: **0x0000000000**
Type: **R/W**

Bit Field	Function Name	Description
39:0	NCO3 Delta Frequency offset	See description of the register at address 0x18D:0x191

Register_Address: **0x1B0**
Register Name: **synth_drive_pll**
Default Value: **0xE4**
Type:R/W

Bit Field	Function Name	Description
7:6	DPLL for Synth 3	Selects DPLL that drives Synthesizer 3 Selection: 00 = DPLL0 01 = DPLL1 10 = DPLL2 11 = DPLL3 **Note:** If this register needs to be changed when external feedback is enabled; please disable external feedback, change the register value then enable external feedback.
5:4	DPLL for Synth 2	See description for bits 7:6
3:2	DPLL for Synth 1	See description for bits 7:6
1:0	DPLL for Synth 0	See description for bits 7:6

Register_Address: **0x1B1**
Register Name: **synth_enable**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3	Synth3 Enable	When this bit is set high, Synthesizer 3 is enabled. When low, Synthesizer 3 is disabled.
2	Synth2 Enable	See description for bit 3
1	Synth1 Enable	See description for bit 3
0	Synth0 Enable	See description for bit 3

Register_Address: **0x1B6**
Register Name: **sync_fail_flag_status**
Default Value: **0x00**
Type: **R**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3	Synth3 APLL sync failure flag status	When high, this bit indicates that Synth3 APLL has lost lock, therefore generating wrong output frequency. This sticky bit is cleared by the **clear_sync_fail_flag** register bit. To check the status, first clear the bit using **clear_sync_fail_flag** register bit 3 for Synth3, then check the bit from this register. Note: This bit will be set upon power up or device reset
2	Synth2 APLL sync failure flag status	See description for bit 3
1	Synth1 APLL sync failure flag status	See description for bit 3
0	Synth0 APLL sync failure Flag status	See description for bit 3

Register_Address: **0x1B7**
Register Name: **clear_sync_fail_flag**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3	Synth3 APLL clear syncfailFlag	When high, this bit clears the syncFailFlag for Synth3 APLL. Note: after clearing the syncFailFlag, this bit MUST be set to low for normal device operation
2	Synth2 APLL clear syncfailFlag	See description for bit 3
1	Synth1 APLL clear syncfailFlag	See description for bit 3
0	Synth0 APLL clear syncfailFlag	See description for bit 3

Register_Address: **0x1B8:0x1B9**
Register Name: **synth0_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth0 base frequency Bs0	Unsigned binary value of these bits represents Synthesizer 0 base frequency Bs in Hz. Examples of values for Bs that can be programmed: 0x1F40 for 8kHz, 0x61A8 for 25kHz, 0x9C40 for 40kHz. **Note 1:** Br has to be directly divisible from 1600000000, i.e. mod (1600000000, Br) has to be 0. The evaluation board GUI can generate recommended Br, Kr, Mr and Nr values for required input frequency. **Note 2:** in order to write e.g. 0x9C40 to this register (and any other register whose value is larger than 8 bits), 0x9C has to be written to the lower address and 0x40 to the upper address (big endian) with the 0x40 (LSBs) written last.

Register_Address: **0x1BA:0x1BB**
Register Name: **synth0_freq_multiple**
Default Value: **0x0798**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth0 base frequency multiple Ks0	Unsigned binary value that represents Synthesizer 0 base frequency multiplication number. For a regular (non-FEC) synthesizer frequency, the 'Base frequency' number Bs is multiplied by the 'Base frequency multiple' number Ks, and multiplied by 16 is equal the synthesizer frequency in Hz. The synthesizer frequency must be programmed to be between 1 GHz and 1.5 GHz, so: Bs x Ks x 16 x Ms / Ns has to be between 1 000 000 000 and 1 500 000 000 Hz. Examples of appropriate values that can be programmed for Bs and Ks to get desired synthesizer frequency: Synthesizer frequency Base frequency Bs Base frequency multiple Ks 1.048576 GHz 8 kHz (0x1F40) 8192 (0x2000) 1.24416 GHz 40 kHz (0x9C40) 1944 (0x0798) 1.25 GHz 25 kHz (0x61A8) 3125 (0x0C35) **Note 1:** Br has to be directly divisible from 1600000000, i.e. mod (1600000000, Br) has to be 0. The evaluation board GUI can generate recommended Br, Kr, Mr and Nr values for required input frequency. **Note 2:** For proper operation of the synthesizer, Bs x Ks x Ms / Ns must not be a multiple any of the following frequencies: 65,536,000; 69,632,000; 73,728,000; 77,824,000; 81,920,000; 86,016,000 or 90,112,000.

Register_Address: **0x1BC:0x1BF**
Register Name: **synth0_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Synth0 FEC ratio numerator Ms0	The unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer 0 FEC multiplication ratio. Synthesizer 0 FEC frequencies are calculated using the following formula: Synth_freq [Hz] = Bs x Ks x 16 x Ms / Ns For regular (non-FEC) synthesizer frequencies, Ms and Ns should be programmed to be 0x0001 Examples of some synthesizer FEC frequencies and appropriate values for Bs, Ks, Ms and Ns registers to get those FEC frequencies are: a) OC-192 mode, standard EFEC for long reach: Desired frequency - 155.52MHz x 255/237 Synth frequency - 1.24416 GHz x 255/237 Base freq. Bs - 40 kHz (0x9C40) Base freq. mul. Ks - 1944 (0x0798) FEC ratio num. Ms - 255 (0x00FF) FEC ratio den. - 237 (0x00ED) Post div PA - 8 b) Long reach 10GE mode, double rate conversion (synth freq : 1250MHz x 66/64 x 255/238): Desired frequency - 156.25MHz x 66/64 x 255/238 Base frequency Bsr - 25 kHz (0x061A8 Base freq mul. Ks - 3125 (0x0C35) FEC ratio num. Ms - 66x255 (0x41BE) FEC ratio den. Ns - 64x238 (0x3B80) Post div PA - 8
15:0	Synth0 FEC ratio denominator Ns0	

Register_Address: **0x1C0:0x1C1**
Register Name: **synth1_base_freq**
Default Value: **0x61A8**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth1 base frequency Bs1	See description for register at address 0x1B8:0x1B9

Register_Address: **0x1C2:0x1C3**
Register Name: **synth1_freq_multiple**
Default Value: **0x0C35**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth1 base frequency multiple Ks1	See description for register at address 0x1BA:0x1BB

Register_Address: **0x1C4:0x1C7**
Register Name: **synth1_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Synth1 FEC ratio numerator Ms1	See description for register at address 0x1BC:0x1BF
15:0	Synth1 FEC ratio denominator Nr1	

Register_Address: **0x1C8:0x1C9**
Register Name: **synth2_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth2 base frequency Bs2	See description for register at address 0x1B8:0x1B9

Register_Address: **0x1CA:0x1CB**
Register Name: **synth2_freq_multiple**
Default Value: **0x0798**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth2 base frequency multiple Ks2	See description for register at address 0x1BA:0x1BB

Register_Address: **0x1CC:0x1CF**
Register Name: **synth2_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Synth2 FEC ratio numerator Ms2	See description for register at address 0x1BC:0x1BF
15:0	Synth2 FEC ratio denominator Nr2	

Register_Address: **0x1D0:0x1D1**
Register Name: **synth3_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth3 base frequency Bs3	See description for register at address 0x1B8:0x1B9

Register_Address: **0x1D2:0x1D3**
Register Name: **synth3_freq_multiple**
Default Value: **0x0798**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth3 base frequency multiple Ks3	See description for register at address 0x1BA:0x1BB

Register_Address: **0x1D4:0x1D7**
Register Name: **synth3_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Synth3 FEC ratio numerator Ms3	See description for register at address 0x1BC:0x1BF
15:0	Synth3 FEC ratio denominator Nr3	

Register_Address: **0x1FF**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Page Selection register	See description for register at address 0x07F

Register_Address: **0x200:0x202**
Register Name: **synth0_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse or clock selection	When these bits are programmed ’1111’ the output clock will be a frame pulse or a low frequency clock (below 1 KHz). Selection between frame pulse and low frequency clock depends on the value of bits 17:16. Low frequency mode: ’1111’ and bits[17:16] == ’00’ : The output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency Bs0 (synth0_base_freq register) divided by the value in bits[15:0] of this register. Frame pulse mode: ’1111’ and bits[17:16] != ’00’ : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] Regular clock mode: If these bits are different from ’1111’ than the output is a clock with 50% duty cycle and frequency equal to the Synthesizer0 frequency (1 GHz to 1.5 GHz) divided by the value in bits [23:0] of this register.
19	Frame pulse type	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’00’ ,this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
18	Frame pulse polarity	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’00’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
17:16	Frame pulse reference clock	Whenever bits[23:20] == ’1111’ these bits select between the low frequency clock and a the frame pulse related output clock (The Frame pulse width will be equal to the period of the related output clock). Otherwise it is used as part of divider ratio (bits[23:0]) Selection: 00: low frequency clock 01: clock 1 (Synth 0 postdivider B) 10: clock 2 (Synth 0 postdivider C) 11: clock 3 (Synth 0 postdivider D)

Register_Address: **0x200:0x202**
Register Name: **synth0_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Division or frame pulse rate	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] ==’1111’ and bits[17:16] != ’00’ these bits represent the number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] ==’1111’ and bits[17:16] == ’00’ these bits represent the division factor for the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency (synth0_base_freq register) divided by the value stored in these bits. Whenever bits[23:20] !=’1111’ the value is these bits is part of the output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0].

Register_Address: **0x203:0x205**
Register Name: **synth0_post_div_B**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse or clock selection	When these bits are programmed ’1111’ the output clock will be a frame pulse or a low frequency clock (below 1 KHz). Selection between frame pulse and low frequency clock depends on the value of bits 17:16. ’1111’ and bits[17:16] == ’01’ : The output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency Bs0 (synth0_base_freq register) divided by the value in bits[15:0] of this register. ’1111’ and bits[17:16] != ’01’ : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] If these bits are different from ’1111’ than the output is a clock with 50% duty cycle and frequency equal to the Synthesizer0 frequency (1 GHz to 1.5 GHz) divided by the value in bits [23:0] of this register.
19	Frame pulse type	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’01’ ,this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse

Register_Address: **0x203:0x205**
Register Name: **synth0_post_div_B**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
18	Frame pulse polarity	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’01’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
17:16	Frame pulse reference clock	Whenever bits[23:20] == ’1111’ these bits select between the low frequency clock and a the frame pulse related output clock (The Frame pulse width will be equal to the period of the related output clock). Otherwise it is used as part of divider ratio (bits[23:0]) Selection: 00: clock 0 (Synth 0 postdivider A) 01: low frequency clock 10: clock 2 (Synth 0 postdivider C) 11: clock 3 (Synth 0 postdivider D)
15:0	Division or frame pulse rate	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] ==’1111’ and bits[17:16] != ’01’ these bits represent the number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] ==’1111’ and bits[17:16] == ’01’ these bits represent the division factor for the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency (synth0_base_freq register) divided by the value stored in these bits. Whenever bits[23:20] !=’1111’ the value is these bits is part of the output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0].

Register_Address: **0x206:0x208**
Register Name: **synth0_post_div_C**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse or clock selection	When these bits are programmed ’1111’ the output clock will be a frame pulse or a low frequency clock (below 1 KHz). Selection between frame pulse and low frequency clock depends on the value of bits 17:16. ’1111’ and bits[17:16] == ’10’ : The output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency Bs0 (synth0_base_freq register) divided by the value in bits[15:0] of this register. ’1111’ and bits[17:16] != ’10’ : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] If these bits are different from ’1111’ than the output is a clock with 50% duty cycle and frequency equal to the Synthesizer0 frequency (1 GHz to 1.5 GHz) divided by the value in bits [23:0] of this register.
19	Frame pulse type	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’10’ ,this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
18	Frame pulse polarity	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’10’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
17:16	Frame pulse reference clock	Whenever bits[23:20] == ’1111’ these bits select between the low frequency clock and a the frame pulse related output clock (The Frame pulse width will be equal to the period of the related output clock). Otherwise it is used as part of divider ratio (bits[23:0]) Selection: 00: clock 0 (Synth 0 postdivider A) 01: clock 1 (Synth 0 postdivider B) 10: low frequency clock 11: clock 3 (Synth 0 postdivider D)

Register_Address: **0x206:0x208**
Register Name: **synth0_post_div_C**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Division or frame pulse rate	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] ==’1111’ and bits[17:16] != ’10’ these bits represent the number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] ==’1111’ and bits[17:16] == ’10’ these bits represent the division factor for the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency (synth0_base_freq register) divided by the value stored in these bits. Whenever bits[23:20] !=’1111’ the value is these bits is part of the output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0].

Register_Address: **0x209:0x20B**
Register Name: **synth0_post_div_D**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse or clock selection	When these bits are programmed ’1111’ the output clock will be a frame pulse or a low frequency clock (below 1 KHz). Selection between frame pulse and low frequency clock depends on the value of bits 17:16. ’1111’ and bits[17:16] == ’11’ : The output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency Bs0 (synth0_base_freq register) divided by the value in bits[15:0] of this register. ’1111’ and bits[17:16] != ’11’ : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] If these bits are different from ’1111’ than the output is a clock with 50% duty cycle and frequency equal to the Synthesizer0 frequency (1 GHz to 1.5 GHz) divided by the value in bits [23:0] of this register.
19	Frame pulse type	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’11’ ,this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse

Register_Address: **0x209:0x20B**
Register Name: **synth0_post_div_D**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
18	Frame pulse polarity	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’11’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
17:16	Frame pulse reference clock	Whenever bits[23:20] == ’1111’ these bits select between the low frequency clock and a the frame pulse related output clock (The Frame pulse width will be equal to the period of the related output clock). Otherwise it is used as part of divider ratio (bits[23:0]) Selection: 00: clock 0 (Synth 0 postdivider A) 01: clock 1 (Synth 0 postdivider B) 10: clock 2 (Synth 0 postdivider C) 11: low frequency clock
15:0	Division or frame pulse rate	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] ==’1111’ and bits[17:16] != ’11’ these bits represent the number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] ==’1111’ and bits[17:16] == ’11’ these bits represent the division factor for the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency (synth0_base_freq register) divided by the value stored in these bits. Whenever bits[23:20] !=’1111’ the value is these bits is part of the output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0].

Register_Address: **0x20C:0x20E**
Register Name: **synth1_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x200:0x202
19	Frame pulse type	See description for the register at address 0x200:0x202
18	Frame pulse polarity	See description for the register at address 0x200:0x202

Register_Address: **0x20C:0x20E**
Register Name: **synth1_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
17:16	Frame pulse related clock selection	See description for the register at address 0x200:0x202
15:0	Frame pulse or divider	See description for the register at address 0x200:0x202

Register_Address: **0x20F:0x211**
Register Name: **synth1_post_div_B**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x203:0x205
19	Frame pulse type	See description for the register at address 0x203:0x205
18	Frame pulse polarity	See description for the register at address 0x203:0x205
17:16	Frame pulse related clock selection	See description for the register at address 0x203:0x205
15:0	Frame pulse or divider	See description for the register at address 0x203:0x205

Register_Address: **0x212:0x214**
Register Name: **synth1_post_div_C**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x206:0x208
19	Frame pulse type	See description for the register at address 0x206:0x208
18	Frame pulse polarity	See description for the register at address 0x206:0x208
17:16	Frame pulse related clock selection	See description for the register at address 0x206:0x208
15:0	Frame pulse or divider	See description for the register at address 0x206:0x208

Register_Address: **0x215:0x217**
Register Name: **synth1_post_div_D**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x209:0x20B
19	Frame pulse type	See description for the register at address 0x209:0x20B
18	Frame pulse polarity	See description for the register at address 0x209:0x20B
17:16	Frame pulse related clock selection	See description for the register at address 0x209:0x20B
15:0	Frame pulse or divider	See description for the register at address 0x209:0x20B

Register_Address: **0x218:0x21A**
Register Name: **synth2_post_div_A**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x200:0x202
19	Frame pulse type	See description for the register at address 0x200:0x202
18	Frame pulse polarity	See description for the register at address 0x200:0x202
17:16	Frame pulse related clock selection	See description for the register at address 0x200:0x202
15:0	Frame pulse or divider	See description for the register at address 0x200:0x202

Register_Address: **0x21B:0x21D**
Register Name: **synth2_post_div_B**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x203:0x205
19	Frame pulse type	See description for the register at address 0x203:0x205
18	Frame pulse polarity	See description for the register at address 0x203:0x205
17:16	Frame pulse related clock selection	See description for the register at address 0x203:0x205
15:0	Frame pulse or divider	See description for the register at address 0x203:0x205

Register_Address: **0x21E:0x220**
Register Name: **synth2_post_div_C**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x206:0x208
19	Frame pulse type	See description for the register at address 0x206:0x208
18	Frame pulse polarity	See description for the register at address 0x206:0x208
17:16	Frame pulse related clock selection	See description for the register at address 0x206:0x208
15:0	Frame pulse or divider	See description for the register at address 0x206:0x208

Register_Address: **0x221:0x223**
Register Name: **synth2_post_div_D**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x209:0x20B
19	Frame pulse type	See description for the register at address 0x209:0x20B
18	Frame pulse polarity	See description for the register at address 0x209:0x20B
17:16	Frame pulse related clock selection	See description for the register at address 0x209:0x20B
15:0	Frame pulse or divider	See description for the register at address 0x209:0x20B

Register_Address: **0x224:0x226**
Register Name: **synth3_post_div_A**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x200:0x202
19	Frame pulse type	See description for the register at address 0x200:0x202
18	Frame pulse polarity	See description for the register at address 0x200:0x202
17:16	Frame pulse related clock selection	See description for the register at address 0x200:0x202
15:0	Frame pulse or divider	See description for the register at address 0x200:0x202

Register_Address: **0x227:0x229**
Register Name: **synth3_post_div_B**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x203:0x205
19	Frame pulse type	See description for the register at address 0x203:0x205
18	Frame pulse polarity	See description for the register at address 0x203:0x205
17:16	Frame pulse related clock selection	See description for the register at address 0x203:0x205
15:0	Frame pulse or divider	See description for the register at address 0x203:0x205

Register_Address: **0x22A:0x22C**
Register Name: **synth3_post_div_C**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x206:0x208
19	Frame pulse type	See description for the register at address 0x206:0x208
18	Frame pulse polarity	See description for the register at address 0x206:0x208
17:16	Frame pulse related clock selection	See description for the register at address 0x206:0x208
15:0	Frame pulse or divider	See description for the register at address 0x206:0x208

Register_Address: **0x22D:0x22F**
Register Name: **synth3_post_div_D**
Default Value: **0x000000**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x209:0x20B
19	Frame pulse type	See description for the register at address 0x209:0x20B
18	Frame pulse polarity	See description for the register at address 0x209:0x20B
17:16	Frame pulse related clock selection	See description for the register at address 0x209:0x20B
15:0	Frame pulse or divider	See description for the register at address 0x209:0x20B

Register_Address: **0x234:0x235**
Register Name: **phase_shift_s0_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth0 Divider C quadrature phase shift	These bits select the quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer0 Post Divider C. Selection: 000 = 0 degrees (no shift) 001 = -45 degrees 010 = -90 degrees 011 = -135 degrees 100 = -180 (or 180) degrees 101 = 135 degrees 110 = 90 degrees 111 = 45 degrees **Note:** Only use the 0b000 selection with 1 Hz output signals
12:0	Synth0 Divider C coarse phase shift	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer0 frequency for all clocks coming from Synthesizer0 Post Divider C (0=no shift, -1= delay output clock for 1 period, 1 = advance output for 1 period, and so on).

Register_Address: **0x236:0x237**
Register Name: **phase_shift_s0_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth 0 Divider D quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth0 Divider D course phase shift	See description for the register at address 0x234:235

Register_Address: **0x23C:0x23D**
Register Name: **phase_shift_s1_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth 1 Divider C quadrature phase shift	See description for the register at address 0x234:235

Register_Address: **0x23C:0x23D**
Register Name: **phase_shift_s1_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	Synth1 Divider C coarse phase shift	See description for the register at address 0x234:235

Register_Address: **0x23E:0x23F**
Register Name: **phase_shift_s1_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth1 Divider D quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth1 Divider D coarse phase shift	See description for the register at address 0x234:235

Register_Address: **0x244:0x245**
Register Name: **phase_shift_s2_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth2 Divider C quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth2 Divider C coarse phase shift	See description for the register at address 0x234:235

Register_Address: **0x246:0x247**
Register Name: **phase_shift_s2_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth2 Divider D quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth2 Divider D coarse phase shift	See description for the register at address 0x234:235

Register_Address: **0x24C:0x24D**
Register Name: **phase_shift_s3_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth3 Divider C quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth3 Divider C coarse phase shift	See description for the register at address 0x234:235

Register_Address: **0x24E:0x24F**
Register Name: **phase_shift_s3_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth3 Divider D quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth3 Divider D course phase shift	See description for the register at address 0x234:235

Register_Address: **0x250**
Register Name: **synth0_fine_phase_shift**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Synth0 fine phase shift	Unsigned binary value of that represents Synthesizer 0 fine phase shift (advancement) in steps of Synthesizer 0 clock period / 256. **Note:** This register controls the fine phase shift for all clocks coming out of the Synthesizer 0 (including all four postdividers)

Register_Address: **0x251**
Register Name: **synth1_fine_phase_shift**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Synth1 fine phase shift	See description for the register at address 0x250

Register_Address: **0x252**
Register Name: **synth2_fine_phase_shift**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Synth2 fine phase shift	See description for the register at address 0x250

Register_Address: **0x253**
Register Name: **synth3_fine_phase_shift**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Synth3 fine phase shift	See description for the register at address 0x250

Register_Address: **0x254**
Register Name: **Synth1_0_stop_clk**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:6	Synth1 Post Divider D stop clock	Setting of these bits will cause Synthesizer 1 Post Divider D to stop clock on either the rising or falling edge. Selection: 00 - 01 = continuous run (stop clock function is disabled) 10 = stop HPOUTCLK3 on the falling edge (stays low) 11 = stop HPOUTCLK3 on the rising edge (stays high)
5:4	Synth1 Post Divider C stop clock	See description for bits 7:6
3:2	Synth0 Post Divider D stop clock	See description for bits 7:6
1:0	Synth0 Post Divider C stop clock	See description for bits 7:6

Register_Address: **0x255** Register Name: **synth3_2_stop_clk** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:6	Synth3 Post Divider D stop clock	See description for register at address 0x254
5:4	Synth3 Post Divider C stop clock	See description for register at address 0x254
3:2	Synth2 Post Divider D stop clock	See description for register at address 0x254
1:0	Synth2 Post Divider C stop clock	See description for register at address 0x254

Register_Address: **0x261** Register Name: **hp_diff_en** Default Value: **0x00** Type:**R/W**		
Bit Field	Function Name	Description
7	enable HPDIFF7	When this bit is set to high, it will enable HPDIFF7_P and HPDIFF7_N outputs. When low, the outputs are tristated.
6	enable HPDIFF6	See description for bit 7
5	enable HPDIFF5	See description for bit 7
4	enable HPDIFF4	See description for bit 7
3	enable HPDIFF3	See description for bit 7
2	enable HPDIFF2	See description for bit 7
1	enable HPDIFF1	See description for bit 7
0	enable HPDIFF0	See description for bit 7

Register_Address: **0x262** Register Name: **hp_cmos_en** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	enable HPOUTCLOCK7	When this bit is set to high, it will enable HPOUTCLK7 output. When low, the output is tristated.
6	enable HPOUTCLOCK6	See description for bit 7
5	enableHPOUTCLOCK5	See description for bit 7
4	enable HPOUTCLOCK4	See description for bit 7

Register_Address: **0x262**
Register Name: **hp_cmos_en**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
3	enable HPOUTCLOCK3	See description for bit 7
2	enable HPOUTCLOCK2	See description for bit 7
1	enable HPOUTCLOCK1	See description for bit 7
0	enable HPOUTCLOCK0	See description for bit 7

Register_Address: **0x266**
Register Name: **gpio_function_pin0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	GPIO0 control or status select	This bit determines whether GPIO0 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status
6:0	GPIO0 table bit address	Unsigned binary value of these bits represent the address in the control or status table, depending on 'GPIO0 control or status select' bit. The GPIO control and status tables are specified in 5.3, “GPIO Configuration“ Default: No function assigned

Register_Address: **0x267**
Register Name: **gpio_function_pin1**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	GPIO1 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO1 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x268**
Register Name: **gpio_function_pin2**
Default Value: **0x60**
Type:**R/W**

Bit Field	Function Name	Description
7	GPIO2 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO2 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x269**
Register Name: **gpio_function_pin3**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	GPIO3 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO3 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x26A**
Register Name: **gpio_function_pin4**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	GPIO4 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO4 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x26B**
Register Name: **gpio_function_pin5**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	GPIO5 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO5 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x26C** Register Name: **gpio_function_pin6** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	GPIO6 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO6 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x276** Register Name: **gpio_in_6_0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	Reserved	Leave as default
6	Input value for GPIO6	Logic values seen on pins GPIO6 when **gpio_function_pin6 ==** 0x00 (control mode and function 0) and the bit for GPIO6 is '0' in **gpio_out_en_6_0**
5	Input value for GPIO5	See description for bit 6
4	Input value for GPIO4	See description for bit 6
3	Input value for GPIO3	See description for bit 6
2	Input value for GPIO2	See description for bit 6
1	Input value for GPIO1	See description for bit 6
0	Input value for GPIO0	See description for bit 6

Register_Address: **0x278** Register Name: **gpio_out_6_0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	Reserved	Leave as default
6	Set GPIO6 output	Sets the output value of GPIO6 when **gpio_function_pin6 ==** 0x00 (status mode and function 0) and the bit for GPIO6 is '1' in **gpio_out_en_6_0**
5	Set GPIO5 output	See description for bit 6
4	Set GPIO4 output	See description for bit 6
3	Set GPIO3 output	See description for bit 6
2	Set GPIO2 output	See description for bit 6

Register_Address: **0x278**
Register Name: **gpio_out_6_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
1	Set GPIO1 output	See description for bit 6
0	Set GPIO0 output	See description for bit 6

Register_Address: **0x27A**
Register Name: **gpio_out_en_6_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6	Enable GPIO6 output	If bit is a '0' and **gpio_function_pin6** is a 0x00, then GPIO6 is an input and data sensed on GPIO6 is reflected in the **gpio_in_6_0** register (bit 6). If bit is a '1' and **gpio_function_pin6** is 0x00, then GPIO6 is an output and the value in **gpio_out_6_0** (bit 6) driven out on GPIO6.
5	Enable GPIO5 output	See description for bit 6
4	Enable GPIO4 output	See description for bit 6
3	Enable GPIO3 output	See description for bit 6
2	Enable GPIO2 output	See description for bit 6
1	Enable GPIO1 output	See description for bit 6
0	Enable GPIO0 output	See description for bit 6

Register_Address: **0x27C**
Register Name: **gpio_latch_6_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	**Reserved**	**Leave as default**
6	Latch GPIO6 input	Set to latch the current value on GPIO6 pin. If this bit is zero, the value in bit 6 of gpio_in_6_0 will change as the logic level on GPIO6 changes.
5	Latch GPIO5 input	See description for bit 6
4	Latch GPIO4 input	See description for bit 6
3	Latch GPIO3 input	See description for bit 6
2	Latch GPIO2 input	See description for bit 6
1	Latch GPIO1 input	See description for bit 6

Register_Address: **0x27C**
Register Name: **gpio_latch_6_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	Latch GPIO0 input	See description for bit 6

Register_Address: **0x27F**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	SPI Page Selection register	Unsigned binary value of these bits represents selected page for SPI access. See register at address 0x07F for details

Register_Address: **0x2C2**
Register Name: **dpll0_fast_lock_ctrl**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:2	Reserved	Leave as default
1	fast_lock_force_en	This is the control to force-enable the fast-lock feature. This control, when enabled, will ignore the frequency and phase error thresholds set in **dpll0_fast_lock_phase_error_threshold** and **dpll0_fast_lock_freq_error_threshold**. Selection: 0 - Normal operation 1 - Force fast-lock mode **Note 1:** The master-control (bit 0 of this register) still has to be enabled for this control to work. **Note 2:** The normal usage for this bit is to set it to 1, then set it back to 0 after waiting per the procedure in “Time between two write accesses to the same register” on page 53.
0	fast_lock_master_enable	This is the master-enable control for the fast-lock feature. 0 - Feature disabled 1 - Feature enabled

Register_Address: **0x2C3**
Register Name: **dpll0_fast_lock_phase_error_threshold**
Default Value: **0xFF**
Type:**R/W**

Bit Field	Function Name	Description
7:0	dpll0_fast_lock_phase_error_thld	This is the phase error threshold for triggering a transition to fast-lock. The threshold is specified in steps of 250ns. If the threshold is programmed to zero, the phase error threshold check is disabled.

Register_Address: **0x2C4**
Register Name: **dpll0_fast_lock_freq_error_threshold**
Default Value: **0x04**
Type:**R/W**

Bit Field	Function Name	Description
7:0	dpll0_fast_lock_freq_error_thld	This is the frequency error threshold for triggering a transition to fast-lock. The threshold is specified in steps of 1ppm, programmable from 1 to 255ppm. If the threshold is programmed to zero, the fast-lock frequency error check is disabled.

Register_Address: **0x2C5**
Register Name: **dpll1_fast_lock_ctrl**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:2	Reserved	Leave as default
1	fast_lock_force_en	See description for register at address 0x2C2 bit 1
0	fast_lock_master_enable	See description for register at address 0x2C2 bit 0

Register_Address: **0x2C6**
Register Name: **dpll1_fast_lock_phase_error_threshold**
Default Value: **0xFF**
Type:**R/W**

Bit Field	Function Name	Description
7:0	dpll1_fast_lock_phase_error_thld	See description for register at address 0x2C3

Register_Address: **0x2C7**
Register Name: **dpll1_fast_lock_freq_error_threshold**
Default Value: **0x04**
Type:**R/W**

Bit Field	Function Name	Description
7:0	dpll1_fast_lock_freq_error_thld	See description for register at address 0x2C4

Register_Address: **0x2C8**
Register Name: **dpll2_fast_lock_ctrl**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:2	Reserved	Leave as default
1	fast_lock_force_en	See description for register at address 0x2C2 bit 1
0	fast_lock_master_enable	See description for register at address 0x2C2 bit 0

Register_Address: **0x2C9**
Register Name: **dpll2_fast_lock_phase_error_threshold**
Default Value: **0xFF**
Type:**R/W**

Bit Field	Function Name	Description
7:0	dpll2_fast_lock_phase_error_thld	See description for register at address 0x2C3

Register_Address: **0x2CA**
Register Name: **dpll2_fast_lock_freq_error_threshold**
Default Value: **0x04**
Type:**R/W**

Bit Field	Function Name	Description
7:0	dpll2_fast_lock_freq_error_thld	See description for register at address 0x2C4

Register_Address: **0x2CB**
Register Name: **dpll3_fast_lock_ctrl**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:2	Reserved	Leave as default
1	fast_lock_force_en	See description for register at address 0x2C2 bit 1
0	fast_lock_master_enable	See description for register at address 0x2C2 bit 0

Register_Address: **0x2CC**
Register Name: **dpll3_fast_lock_phase_error_threshold**
Default Value: **0xFF**
Type:**R/W**

Bit Field	Function Name	Description
7:0	dpll2_fast_lock_phase_error_thld	See description for register at address 0x2C3

Register_Address: **0x2CD**
Register Name: **dpll3_fast_lock_freq_error_threshold**
Default Value: **0x04**
Type:**R/W**

Bit Field	Function Name	Description
7:0	dpll3_fast_lock_freq_error_thld	See description for register at address 0x2C4

Register_Address: **0x2CE**
Register Name: **dpll_fast_lock_error_status**
Default Value: **0x00**
Type:**StickyR/W**

Bit Field	Function Name	Description
7	DPLL3_freq_error_status	This status bit indicates if the frequency error threshold for DPLL3 has been exceeded. This status bit will work only if the frequency error threshold check has been enabled (i.e. the frequency error threshold has been programmed to a non-zero value). This bit is 'sticky', so it will stay high until customer clears it.
6	DPLL3_phase_error_status	This status bit indicates if the phase error threshold for DPLL3 has been exceeded. This status bit will work only if the phase error threshold check has been enabled (i.e. the phase error threshold has been programmed to a non-zero value). This bit is 'sticky', so it will stay high until customer clears it.

Register_Address: **0x2CE**
Register Name: **dpll_fast_lock_error_status**
Default Value: **0x00**
Type:**StickyR/W**

Bit Field	Function Name	Description
5	DPLL2_freq_error_status	This status bit indicates if the frequency error threshold for DPLL2 has been exceeded. This status bit will work only if the frequency error threshold check has been enabled (i.e. the frequency error threshold has been programmed to a non-zero value). This bit is 'sticky', so it will stay high until customer clears it.
4	DPLL2_phase_error_status	This status bit indicates if the phase error threshold for DPLL2 has been exceeded. This status bit will work only if the phase error threshold check has been enabled (i.e. the phase error threshold has been programmed to a non-zero value). This bit is 'sticky', so it will stay high until customer clears it.
3	DPLL1_freq_error_status	This status bit indicates if the frequency error threshold for DPLL1 has been exceeded. This status bit will work only if the frequency error threshold check has been enabled (i.e. the frequency error threshold has been programmed to a non-zero value). This bit is 'sticky', so it will stay high until customer clears it.
2	DPLL1_phase_error_status	This status bit indicates if the phase error threshold for DPLL1 has been exceeded. This status bit will work only if the phase error threshold check has been enabled (i.e. the phase error threshold has been programmed to a non-zero value). This bit is 'sticky', so it will stay high until customer clears it.
1	DPLL0_freq_error_status	This status bit indicates if the frequency error threshold for DPLL0 has been exceeded. This status bit will work only if the frequency error threshold check has been enabled (i.e. the frequency error threshold has been programmed to a non-zero value). This bit is 'sticky', so it will stay high until customer clears it.
0	DPLL0_phase_error_status	This status bit indicates if the phase error threshold for DPLL0 has been exceeded. This status bit will work only if the phase error threshold check has been enabled (i.e. the phase error threshold has been programmed to a non-zero value). This bit is 'sticky', so it will stay high until customer clears it.

Register_Address: **0x2CF**
Register Name: **dpll_fcl_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:6	DPLL3 FCL Control	This register enables the frequency change limiter based on manual or automatic control. If automatic mode is selected, then the operation of FCL depends on the bandwidth. If BW<= 0.1Hz, then FCL is enabled. For other bandwidths, FCL is disabled. Selection: 00 -FCL automatic 01- FCL disabled 10 -FCL enabled 11 -FCL disabled
5:4	DPLL2 FCL Control	This register enables the frequency change limiter based on manual or automatic control. If automatic mode is selected, then the operation of FCL depends on the bandwidth. If BW<= 0.1Hz, then FCL is enabled. For other bandwidths, FCL is disabled. Selection: 00 -FCL automatic 01- FCL disabled 10 -FCL enabled 11 -FCL disabled
3:2	DPLL1 FCL Control	This register enables the frequency change limiter based on manual or automatic control. If automatic mode is selected, then the operation of FCL depends on the bandwidth. If BW<= 0.1Hz, then FCL is enabled. For other bandwidths, FCL is disabled. Selection: 00 -FCL automatic 01- FCL disabled 10 -FCL enabled 11 -FCL disabled

Register_Address: **0x2CF**
Register Name: **dpll_fcl_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
1:0	DPLL0 FCL Control	This register enables the frequency change limiter based on manual or automatic control. If automatic mode is selected, then the operation of FCL depends on the bandwidth. If BW<= 0.1Hz, then FCL is enabled. For other bandwidths, FCL is disabled. Selection: 00 -FCL automatic 01- FCL disabled 10 -FCL enabled 11 -FCL disabled

Register_Address: **0x2D4**
Register Name: **dpll0_holdover_filt_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Holdover Filter Value	This register specifies the holdover filter bandwidth. The default value of 0x00 means that the filter is bypassed. These are the possible settings (BW = 343/(2^n*2*pi) Hz): Setting BW 0x00 Bypass (default) 0x01 27.3 Hz 0x02 13.6 Hz 0x03 6.8 Hz 0x04 3.4 Hz 0x05 1.7 Hz 0x06 883 mHz 0x07 426 mHz 0x08 213 mHz 0x09 107 mHz 0x0A 53.3 mHz 0x0B 26.6 mHz 0x0C 13.3 mHz 0x0D 6.7 mHz 0x0E 3.3 mHz 0x0F 1.7 mHz

Register_Address: **0x2D5**
Register Name: **dpll1_holdover_filt_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Holdover Filter Value	See description for register at address 0x2D4

Register_Address: **0x2D6**
Register Name: **dpll2_holdover_filt_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Holdover Filter Value	See description for register at address 0x2D4

Register_Address: **0x2D7**
Register Name: **dpll3_holdover_filt_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Holdover Filter Value	See description for register at address 0x2D4

Register_Address: **0x2D8**
Register Name: **dpll0_nco_ref_switch_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default

Register_Address: **0x2D8**
Register Name: **dpll0_nco_ref_switch_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	DPLL0 NCO Ref-switch Control	Controls whether fast-lock is forcibly disabled during transitions out of NCO mode. Selection: 0: Fast-lock is disabled during transitions out of NCO mode 1: Fast-lock is allowed during transitions out of NCO mode

Register_Address: **0x2D9**
Register Name: **dpll1_nco_ref_switch_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	DPLL1 NCO Ref-switch Control	See description for register at address 0x2D8

Register_Address: **0x2DA**
Register Name: **dpll2_nco_ref_switch_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	DPLL2 NCO Ref-switch Control	See description for register at address 0x2D8

Register_Address: **0x2DB**
Register Name: **dpll3_nco_ref_switch_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default

Register_Address: **0x2DB**
Register Name: **dpll3_nco_ref_switch_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	DPLL3 NCO Ref-switch Control	See description for register at address 0x2D8

Register_Address: **0x2DC**
Register Name: **dpll0_lock_delay**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL0 Lock Delay	This register specifies additional delay before lock is declared. Delay time (s) = **dpll0_lock_delay**^2 for a range of 0 to 65025 seconds.

Register_Address: **0x2DD**
Register Name: **dpll1_lock_delay**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL1 Lock Delay	See description for register at address 0x2DC

Register_Address: **0x2DE**
Register Name: **dpll2_lock_delay**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL2 Lock Delay	See description for register at address 0x2DC

Register_Address: **0x2DF**
Register Name: **dpll3_lock_delay**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL3 Lock Delay	See description for register at address 0x2DC

Register_Address: **0x2E0**
Register Name: **dpll0_fp_lock_criteria**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL0 Lock Criteria	If this register is zero, then frame pulse alignment will not be taken into consider as a lock criteria (diabled). If this register is non-zero, this regisiter specifies the alignment threshold for when a frame pulse should be considered locked. The alignment is the difference between the actual frame pulse position and the expected position. Lock criteria (ns) **= dpll0_fp_lock_criteria*** 100

Register_Address: **0x2E1**
Register Name: **dpll1_fp_lock_criteria**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL1 Lock Criteria	See description for register at address 0x2E0

Register_Address: **0x2E2**
Register Name: **dpll2_fp_lock_criteria**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL2 Lock Criteria	See description for register at address 0x2E0

Register_Address: **0x2E3**
Register Name: **dpll3_fp_lock_criteria**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	DPLL3 Lock Delay	See description for register at address 0x2E0

Register_Address: **0x2E4**
Register Name: **ref0_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref0 Sync Offset Compensation	This 8-bit signed 2's complement value specifies the compensation for the constant offset between the input sync reference (on reference 0) and the associated input clock reference. sync offset (ns) = **ref0_sync_offset_comp***0.5 for a range of -64ns to + 63.5ns.

Register_Address: **0x2E5**
Register Name: **ref1_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref1 Sync Offset Compensation	See description for register at address 0x2E4

Register_Address: **0x2E6**
Register Name: **ref2_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref2 Sync Offset Compensation	See description for register at address 0x2E4

Register_Address: **0x2E7**
Register Name: **ref3_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref3 Sync Offset Compensation	See description for register at address 0x2E4

Register_Address: **0x2E8**
Register Name: **ref4_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref4 Sync Offset Compensation	See description for register at address 0x2E4

Register_Address: **0x2E9**
Register Name: **ref5_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref5 Sync Offset Compensation	See description for register at address 0x2E4

Register_Address: **0x2EA**
Register Name: **ref6_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref6 Sync Offset Compensation	See description for register at address 0x2E4

Register_Address: **0x2EB**
Register Name: **ref7_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref7 Sync Offset Compensation	See description for register at address 0x2E4

Register_Address: **0x2EC**
Register Name: **ref8_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref8 Sync Offset Compensation	See description for register at address 0x2E4

Register_Address: **0x2ED**
Register Name: **ref9_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref9 Sync Offset Compensation	See description for register at address 0x2E4

Register_Address: **0x2EE**
Register Name: **ref10_sync_offset_comp**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Ref10 Sync Offset Compensation	See description for register at address 0x2E4

Register_Address: **0x2FA**
Register Name: **dpll0_ref_sync_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	DPLL0 Frame Sync Alignment Interval	This field specifies the interval in seconds for periodic realignment. If programmed to zero, the alignment is one-shot.
0	DPLL0 Frame Sync Manual Alignment Control	The host sets this bit to start a manual ref-sync alignment process. The device clears the bit to indicate that it started the ref-sync alignment process. **Note:** After this bit is cleared by the host, there may be additional time before the alignment is complete..

Register_Address: **0x2FB**
Register Name: **dpll1_ref_sync_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	DPLL1 Frame Sync Alignment Interval	See description for register at address 0x2FA bits 7:1
0	DPLL1 Frame Sync Manual Alignment Control	See description for register at address 0x2FA bit 0

Register_Address: **0x2FC**
Register Name: **dpll2_ref_sync_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	DPLL2 Frame Sync Alignment Interval	See description for register at address 0x2FA bits 7:1
0	DPLL2 Frame Sync Manual Alignment Control	See description for register at address 0x2FA bit 0

Register_Address: **0x2FD**
Register Name: **dpll3_ref_sync_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:1	DPLL3 Frame Sync Alignment Interval	See description for register at address 0x2FA bits 7:1
0	DPLL3 Frame Sync Manual Alignment Control	See description for register at address 0x2FA bit 0

Register_Address: **0x2FF**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	SPI Page Selection register	Unsigned binary value of these bits represents selected page for SPI access. See register at address 0x07F for details

9.0 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Core supply voltage	V_{CORE_R}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on osci and osco pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Storage temperature	T_{ST}	-55	125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

	Characteristics	Sym	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}	3.135	3.30	3.465	V
2	Core supply voltage	V_{CORE}	1.71	1.80	1.89	V
3	Operating temperature	T_A	-40	25	85	°C
4	Input voltage	V_{DD-IN}	2.97	3.30	3.63	V

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics - Power - Core

	Characteristics	Sym	Typ.	Units	Notes
1	Core supply current (Vcore)	I_{CORE} (V_{DD} 3.3V)	75	mA	
		I_{CORE} (V_{CORE} 1.8V)	242	mA	
2	Current for each HP Synthesis Engine	I_{SYN} (V_{DD} 3.3V)	54	mA	
		I_{SYN}(V_{CORE} 1.8V)	8	mA	

DC Electrical Characteristics - Power - Clock Outputs

	Characteristics	Sym.	Typ.	Units	Notes
1	Power for each hpdiff clock driver	$P_{hpdiff}(V_{DD}$ 3.3V)	89	mW	Including power to biasing and load resistors
2	Power for each hpdiff clock driver minus power dissipated in the biasing and load resistors.	$P_{hpdiff}(V_{DD}$ 3.3V)	49	mW	Without power to biasing and load resistors
3	Power for each hpoutclk clock driver	$P_{hpout}(V_{DD}$ 3.3V)	23	mW	C_L = 5 pf f_{out} = 20 MHz

DC Electrical Characteristics - Inputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage	V_{CIH}	$0.7 \cdot V_{DD}$			V	Excluding pins below
2	CMOS low-level input voltage	V_{CIL}			$0.3 \cdot V_{DD}$	V	Excluding pins below
3	CMOS Input leakage current	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
4	Schmitt high-level input voltage for tck, pwr_b, sck_scl, trst_b	V_{SIH}	2.0			V	
5	Schmitt low-level input voltage for tck, pwr_b, sck_scl, trst_b	V_{SIL}			0.7	V	
6	Differential input common mode voltage	V_{CM}	1.1		2.0	V	
7	Differential input voltage difference	V_{ID}	0.25		1.0	V	

AC/DC Electrical Characteristics - Master Clock Inputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage (OSCi_3V3)	V_{CIH}	$0.7 \cdot V_{DD}$			V	
2	CMOS low-level input voltage (OSCi_3V3)	V_{CIL}			$0.3 \cdot V_{DD}$	V	
3	Input leakage current (OSCi_3V3)	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
4	CMOS high-level input voltage (OSCi_1V8)	V_{CIH}	1.37			V	
5	CMOS low-level input voltage (OSCi_1V8)	V_{CIL}			0.59	V	
6	Input leakage current (OSCi_1V8)	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
7	CMOS high-level input voltage (XOin)	V_{CIH}	2.0			V	

AC/DC Electrical Characteristics - Master Clock Inputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
8	CMOS low-level input voltage (XOin)	V_{CIL}			0.8	V	
9	Input leakage current (XOin)	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
10	Duty Cycle		40		60	%	

DC Electrical Characteristics - High Performance Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	HPCMOS High-level output voltage	V_{OH}	$0.8*V_{DD}$			V	22 Ohms in series C_L = 10 pF
2	HPCMOS Low-level output voltage	V_{OL}			$0.2*V_{DD}$	V	22 Ohms in series C_L = 10 pF
3	LVPECL: High-level output voltage	V_{OH_LVPECL}	V_{DD}- 1.16		V_{DD}- 0.88	V	R_L = 50Ω to V_{DD} - 2V, C_L = 1pF
4	LVPECL: Low-level output voltage	V_{OL_LVPECL}	V_{DD}- 1.81		V_{DD}- 1.55	V	R_L = 50Ω to V_{DD} - 2V, C_L = 1pF
5	LVPECL: Differential output voltage*	V_{OD_LVPECL}	0.38		0.94	V	R_L = 50Ω to V_{DD} - 2V, C_L = 1pF

* IBIS model should be used to estimate differential output voltage for different trace lengths and different output frequencies.

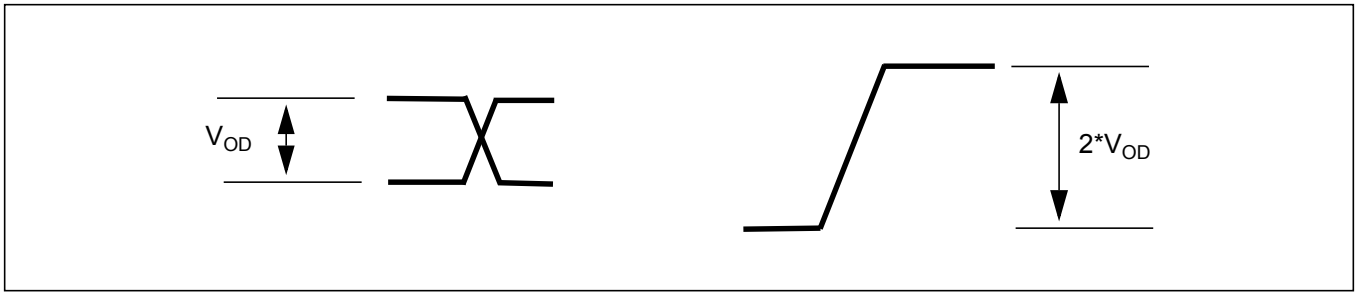


Figure 26 - Timing Parameter - Output Differential

AC Electrical Characteristics* -Output Timing Parameters Measurement Voltage Levels (see Figure 27)

	Characteristics	Sym.	CMOS	LVPECL	Units
1	Threshold Voltage	$V_{T\text{-}CMOS}$ $V_{T\text{-}LVPECL}$	$0.5V_{DD}$	V_{DD}-1.35	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.8V_{DD}$	$0.8V_{OD\_LVPECL}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.2V_{DD}$	$0.2V_{OD\_LVPECL}$	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated

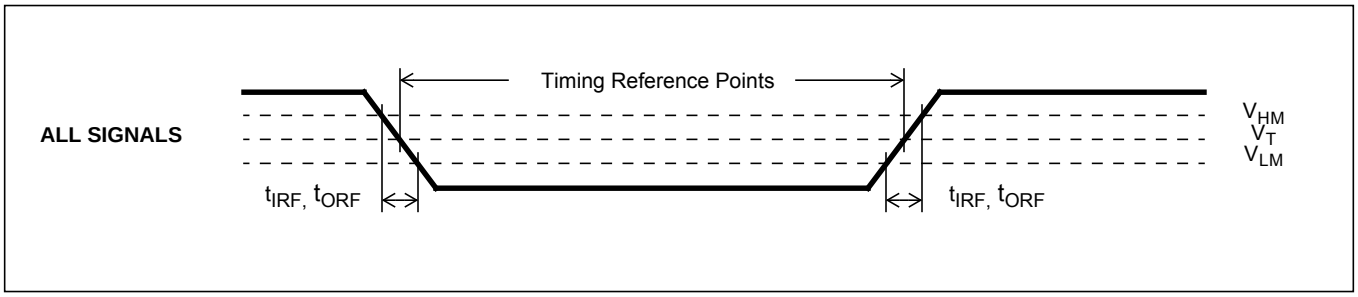


Figure 27 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics* - Inputs (see Figure 28 and Figure 29).

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Input reference Frequency (CMOS Inputs)	$1/t_{REFP}$			177.5	MHz
2	Input reference Frequency (LVPECL Inputs)	$1/t_{REFP}$			750	MHz
3	Input reference pulse width high or low	t_{REFW}	0.55			ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions

AC Electrical Characteristics* - Input To Output Timing (see Figure 28 and Figure 29)

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Input reference to hpoutclk0 (single-ended) output clock (with same frequency) delay	t_{HP_REFD}	-2	0	2	ns
2	Input reference to hpdiff0 (differential) output clock (with same frequency) delay	$t_{HP\_DIFF\_REFD}$	-1.2	0	1.6	ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

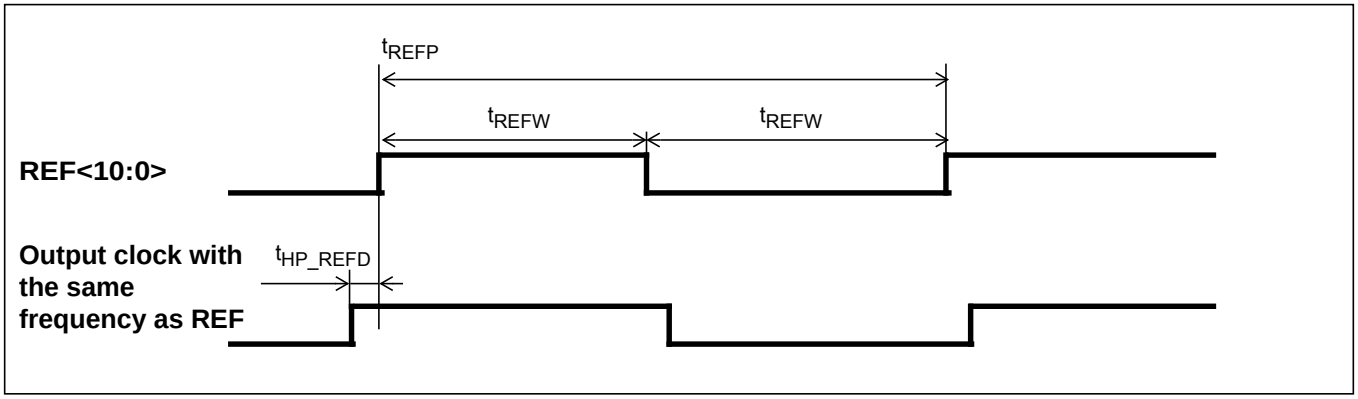


Figure 28 - Input To Output Timing for hpoutclk0

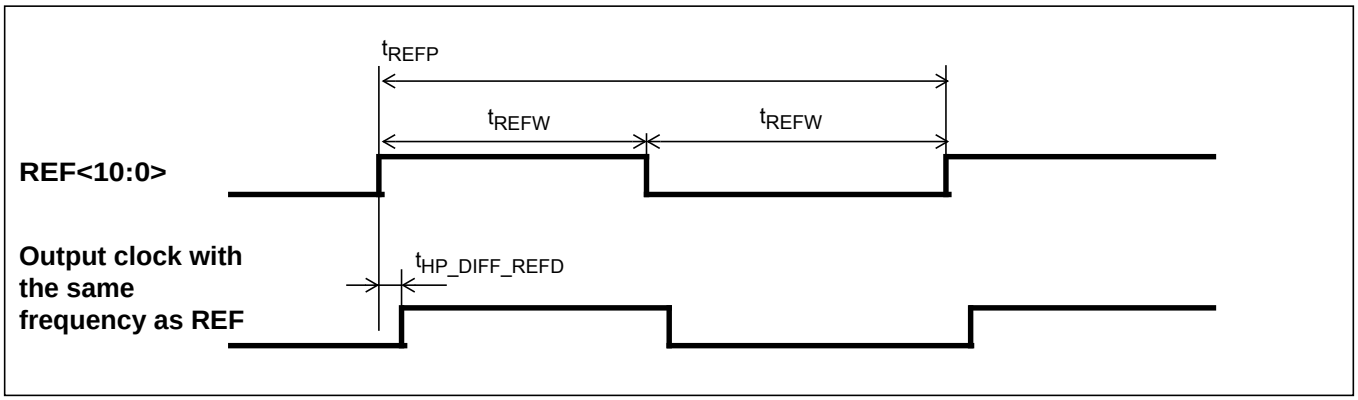


Figure 29 - Input To Output Timing To hpdiff0_P/N

AC Electrical Characteristics* - Input Timing For Sync References (See Figure 30)

	Characteristics	Symbol	Min.	Typical	Max.	Units	Notes
1	sync lead time	t_{SYNC_LD}	0		$t_{REFP}/2 - t_{UNCERT}$	ns	t_{REFP} = minimum period of ref clock
2	sync lag time	t_{SYNC_LG}	0		$t_{REFP}/2 - t_{UNCERT}$	ns	t_{REFP} = minimum period of ref clock
3	sync alignment uncertainty	t_{UNCERT}		2		ns	

.

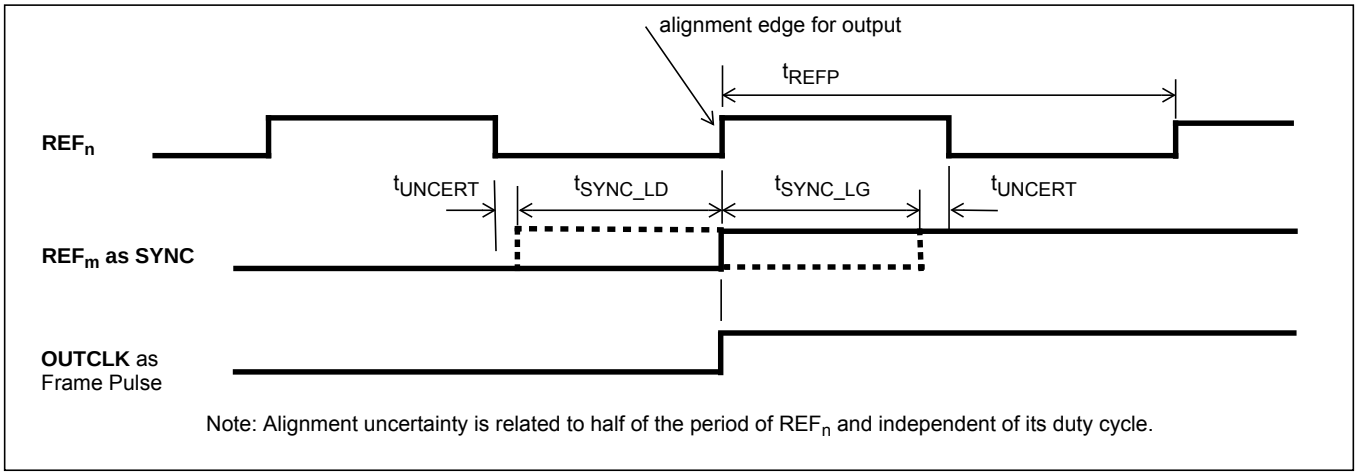


Figure 30 - Sync Input Timing

AC Electrical Characteristics* - Outputs (see Figure 31).

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Clock skew between high performance outputs	$t_{OUT2OUTD}$	-2	0	-2	ns	
2	Output clock Duty Cycle - hpdiff	t_{PWH}, t_{PWL}	45	50	55	Duty Cycle	R_L = 50Ω to V_{DD} - 2V, C_L = 1pF
3	Output clock Duty Cycle - hpoutclkl	t_{PWH}, t_{PWL}	40	50	60	Duty Cycle	22 Ohms in series C_L = 10 pF
4	hpdiff (LVPECL) Output clock rise or fall time	t_r / t_f	265		515	ps	
5	hpoutclk (LVCMOS) clock rise and fall time	t_r / t_f	620		1490	ps	10pF load
6	Output Clock Frequency (hpdiff)	f_{hpdiff}			750	MHz	
7	Output Clock Frequency (hpoutclk)	f_{hpout}			177.5	MHz	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

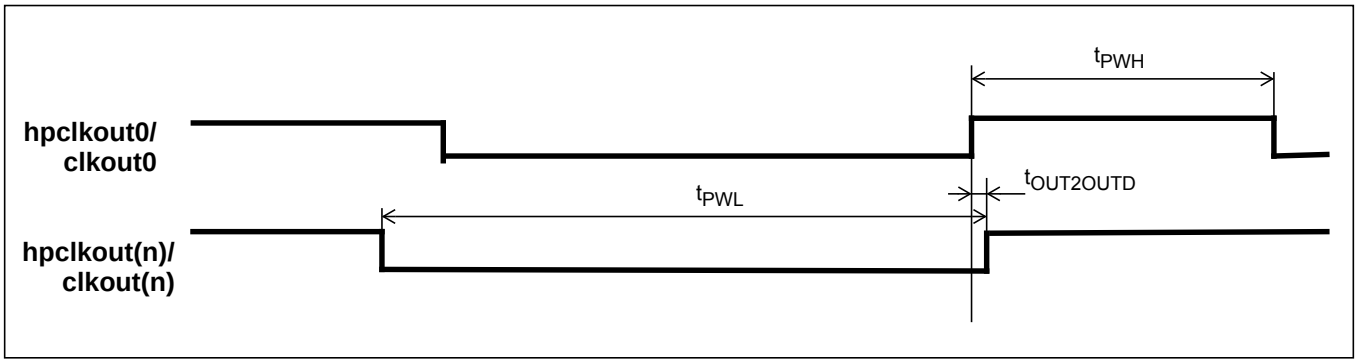


Figure 31 - Output Timing Referenced To hpclkout0/clkout0

Functional waveforms and timing characteristics for the LSB first mode are shown in Figure 32, and Figure 33 describe the MSB first mode. Table 9 shows the timing specifications.

Specification	Name	Min.	Max.	Units
sck period	tcyc	124		ns
sck pulse width low	tclkl	62		ns
sck pulse width high	tclkh	62		ns
si setup (write) from sck rising	trxs	10		ns
si hold (write) from sck rising	trxh	10		ns
so delay (read) from sck falling	txd		25	ns
cs_b setup from sck falling (LSB first)	tcssi	20		ns
cs_b setup from sck rising (MSB first)	tcssm	20		ns
cs_b hold from sck falling (MSB first)	tcshm	10		ns
cs_b hold from sck rising (LSB first)	tcshi	10		ns
cs_b to output high impedance	tohz		60	ns

Table 9 - Serial Peripheral Interface Timing

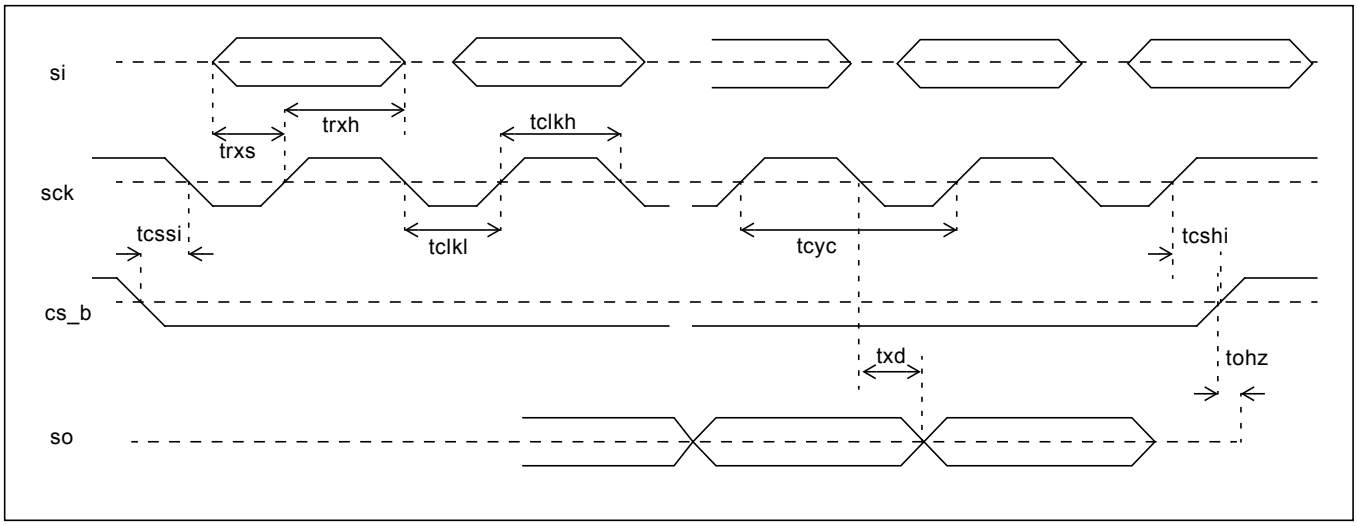


Figure 32 - Serial Peripheral Interface Timing - LSB First Mode

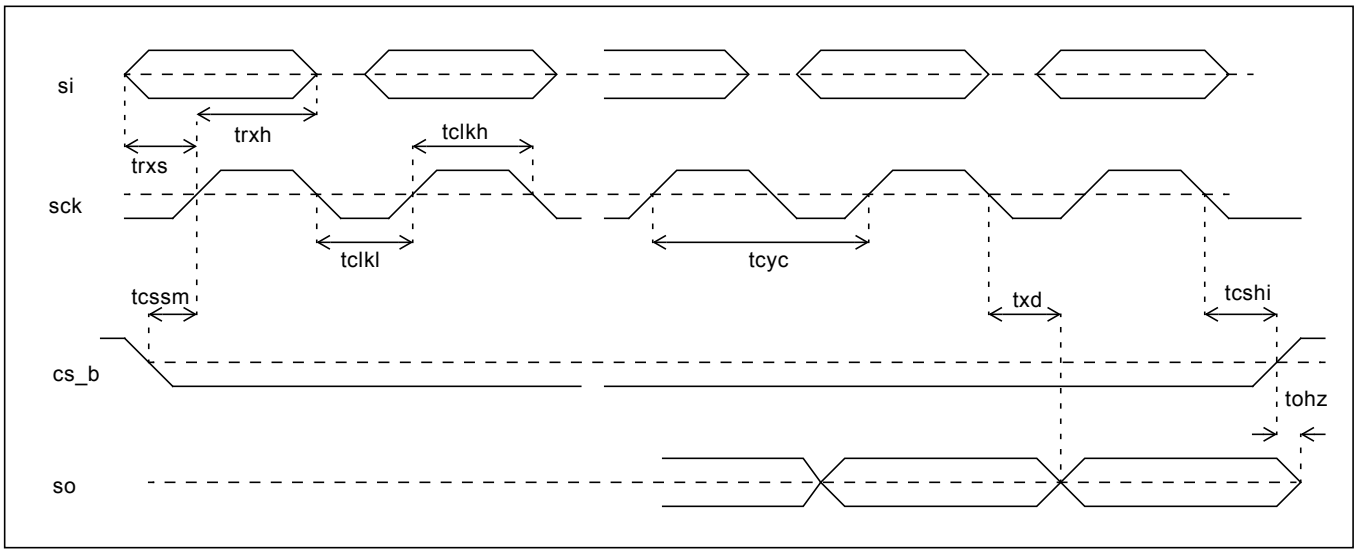


Figure 33 - Serial Peripheral Interface Timing - MSB First Mode

The timing specification for the I^2C interface is shown in Figure 34 and Table 10.

Specification	Name	Min.	Typ.	Max.	Units	Note
SCL clock frequency	f_{SCL}	0		400	kHz	
Hold time START condition	$t_{HD:STA}$	0.6			us	
Low period SCL	t_{LOW}	1.3			us	
Hi period SCL	t_{HIGH}	0.6			us	
Setup time START condition	$t_{SU:STA}$	0.6			us	
Data hold time	$t_{HD:DAT}$	0		0.9	us	
Data setup time	$t_{SU:DAT}$	100			ns	
Rise time	t_r				ns	Determined by choice of pull-up resistor
Fall time	t_f	20 + $0.1C_b$		250	ns	
Setup time STOP condition	$t_{SU:STO}$	0.6			us	
Bus free time between STOP/START	t_{BUF}	1.3			us	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	
Max capacitance for each I/O pin				10	pF	

Table 10 - I^2C Serial Microport Timing

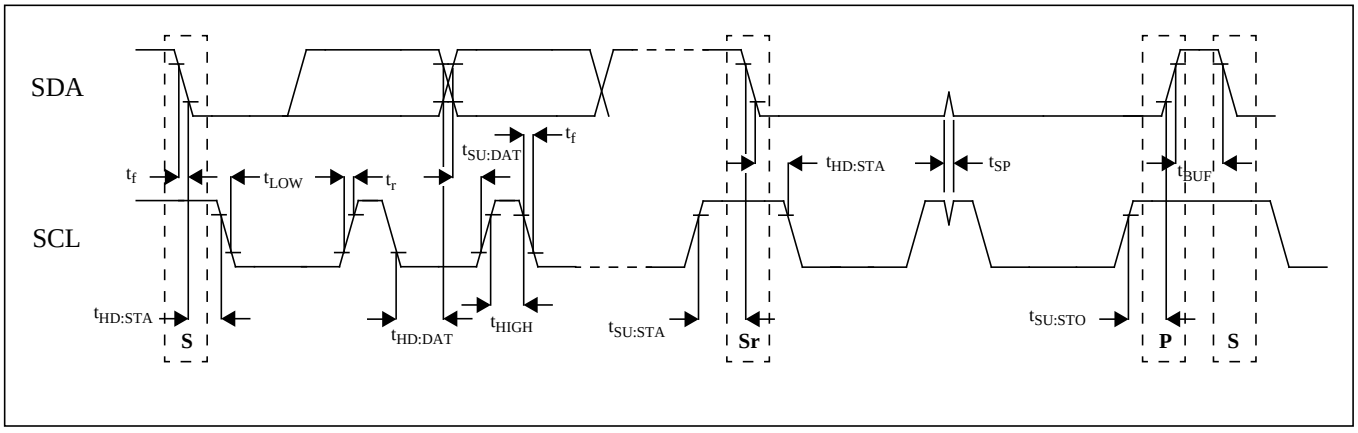


Figure 34 - I^2C Serial Microport Timing

10.0 Performance Characterization

10.1 Output Clocks Jitter Generation

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
622.08 MHz	50 kHz - 80 MHz	0.61	ps_{rms}	
	12 kHz - 20 MHz	0.68	ps_{rms}	

Table 11 - Jitter Generation Specifications - LVPECL Differential (HPDIFF) Outputs

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
25 MHz	12 kHz - 5 MHz	0.73	ps_{rms}	
77.76 MHz	12 kHz - 20 MHz	1.07	ps_{rms}	
125 MHz	12 kHz - 20 MHz	1.07	ps_{rms}	
156.25 MHz	12 kHz - 20 MHz	0.93	ps_{rms}	

Table 12 - Jitter Generation Specifications - LVCMOS Single-ended (HPOUT) Outputs

10.2 DPLL Performance Characteristics

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Pull-in/Hold-in Range	+/-12		+/-2300	ppm	user selectable
2	Lock Time			2	sec	For bandwidths of 5.2 Hz and above and no phase slope limiting
				50	sec	For a bandwidth of 3.6 Hz and PSL of 7.5 microseconds/s
				50	sec	For a bandwidth of 0.1 Hz and PSL of 0.885 microseconds/s
				300	sec	For a bandwidth of 1 mHz and PSL of 0.885 microseconds/s
3	Reference Switching MTIE			5	nsec	
4	Entry into Holdover MTIE			5	nsec	
5	Exit from Holdover MTIE			5	nsec	When bandwidth is not changed during HO
6	Holdover Accuracy			1	ppb	For bandwidths from 0.1 Hz
				10	ppb	For bandwidths from 1.8 Hz to 10 Hz
7	Phase gain in the passband			0.1	dB	

Table 13 - DPLL Characteristics

11.0 Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	Still Air 1 m/s 2 m/s	21.3 19.0 17.8	^{o}C/W

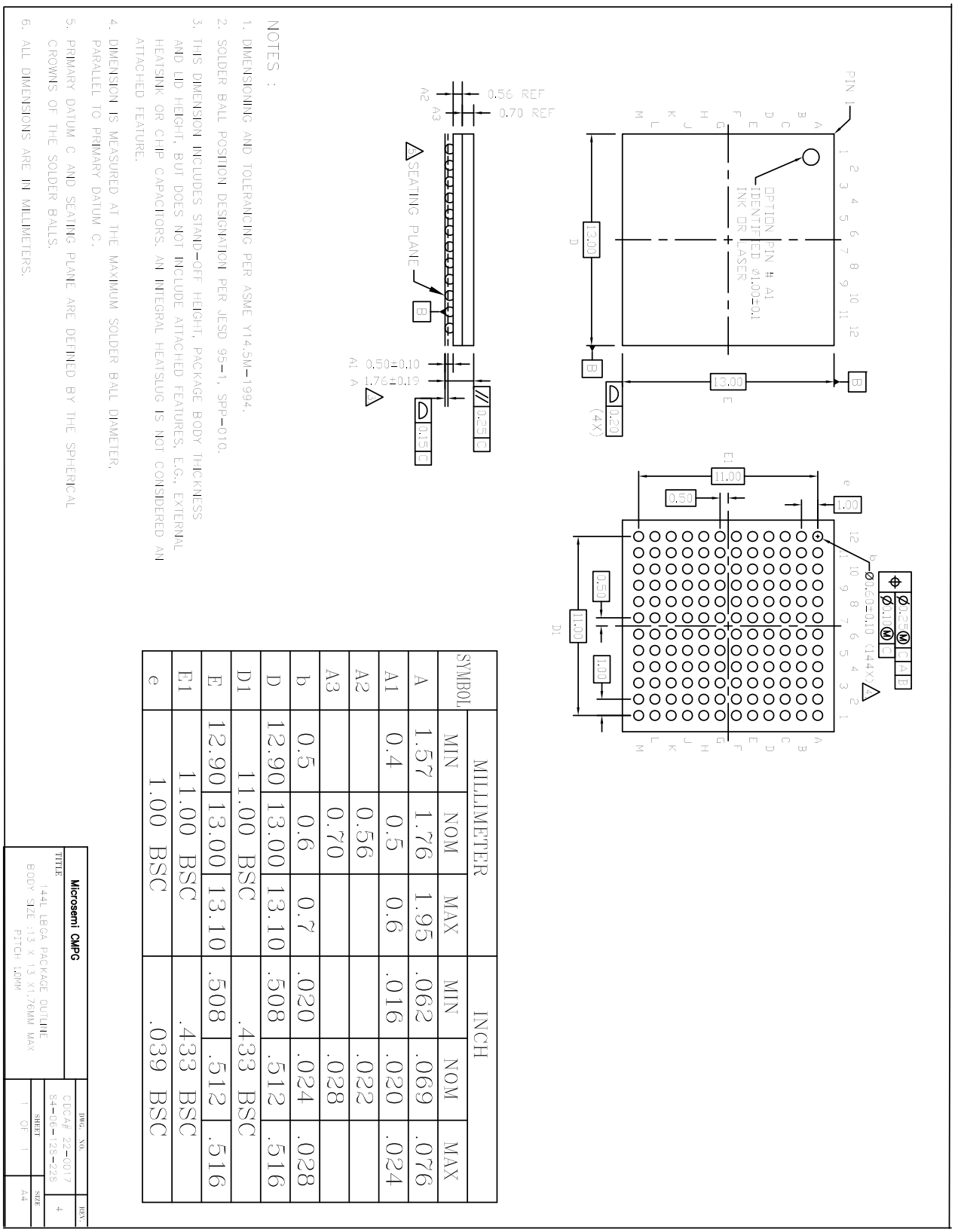
Table 14 - Thermal Care

Parameter	Symbol	Test Condition	Value	Unit
Junction to Case Thermal Resistance	θ_{JC}		4.2	^{o}C/W
Junction to Board Thermal Resistance	θ_{JB}		10.1	^{o}C/W
Maximum Junction Temperature*	T_{jmax}		125	^{o}C
Maximum Ambient Temperature	T_{A}		85	^{o}C

Table 14 - Thermal Care

* Proper thermal management must be practiced to ensure that T_{jmax} is not exceeded.

12.0 Mechanical Drawing



NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
3. THIS DIMENSION INCLUDES STAND-OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.57	1.76	1.95	.062	.069	.076
A1	0.4	0.5	0.6	.016	.020	.024
A2		0.56			.022	
A3		0.70			.028	
b	0.5	0.6	0.7	.020	.024	.028
D	12.90	13.00	13.10	.508	.512	.516
D1		11.00 BSC			.433 BSC	
E	12.90	13.00	13.10	.508	.512	.516
E1		11.00 BSC			.433 BSC	
e		1.00 BSC			.039 BSC	

Microsemi CMPG		DWG. NO	REV
TITTLE: 144L LBGA PACKAGE OUTLINE 13 X 13 X1.76MM MAX BODY SIZE PITCH 1.00MM		CDCA# 22-0017 S4-06-128-225	4
		SHEET 1 OF 1	SIZE A4

13.0 Package Markings

13.1 144-pin BGA. Package Top Mark Format

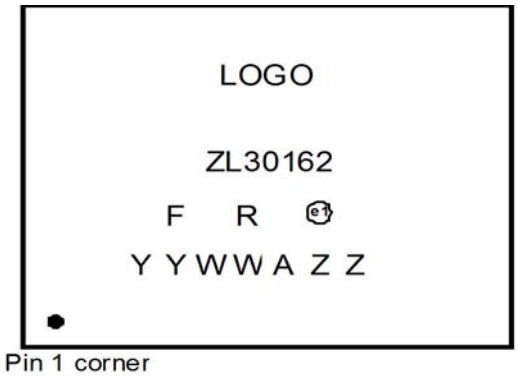


Figure 35 - Non-customized Device Top Mark

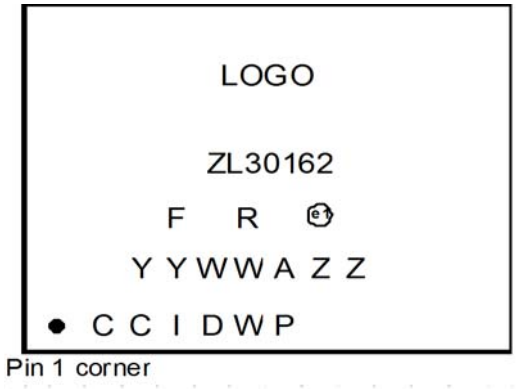


Figure 36 - Custom Factory Programmed Device Top Mark

Line	Characters	Description
1	ZL30162	Part Number
2	F	Fab Code
2	R	Product Revision Code
2	e1	Denotes Pb-Free Package
3	YY	Last Two Digits of the Year of Encapsulation
3	WW	Work Week of Assembly
3	A	Assembly Location Code
3	ZZ	Assembly Lot Sequence
4	CCID	Custom Programming Identification Code
4	WP	Work Week of Programming

Table 15 - Package Marking Legend

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CA 92656 USA

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Sales: +1 (949) 380-6136
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E-mail: sales.support@microsemi.com

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